



# THE LEAD FREE ELECTRONICS MANHATTAN PROJECT – PHASE I

PRESENTED BY  
THE BENCHMARKING AND BEST PRACTICES  
CENTER OF EXCELLENCE



Report Documentation Page				Form Approved OMB No. 0704-0188	
Public reporting burden for the collection of information is estimated to average 1 hour per response, including the time for reviewing instructions, searching existing data sources, gathering and maintaining the data needed, and completing and reviewing the collection of information. Send comments regarding this burden estimate or any other aspect of this collection of information, including suggestions for reducing this burden, to Washington Headquarters Services, Directorate for Information Operations and Reports, 1215 Jefferson Davis Highway, Suite 1204, Arlington VA 22202-4302. Respondents should be aware that notwithstanding any other provision of law, no person shall be subject to a penalty for failing to comply with a collection of information if it does not display a currently valid OMB control number.					
1. REPORT DATE <b>30 JUL 2009</b>		2. REPORT TYPE		3. DATES COVERED <b>00-00-2009 to 00-00-2009</b>	
4. TITLE AND SUBTITLE <b>The Lead Free Electronics Manhattan Project --- Phase I</b>				5a. CONTRACT NUMBER	
				5b. GRANT NUMBER	
				5c. PROGRAM ELEMENT NUMBER	
6. AUTHOR(S)				5d. PROJECT NUMBER	
				5e. TASK NUMBER	
				5f. WORK UNIT NUMBER	
7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES) <b>ACI Technologies Inc,1 International Plaza Suite 600,Philadelphia,PA,19113</b>				8. PERFORMING ORGANIZATION REPORT NUMBER	
9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)				10. SPONSOR/MONITOR'S ACRONYM(S)	
				11. SPONSOR/MONITOR'S REPORT NUMBER(S)	
12. DISTRIBUTION/AVAILABILITY STATEMENT <b>Approved for public release; distribution unlimited</b>					
13. SUPPLEMENTARY NOTES					
14. ABSTRACT					
15. SUBJECT TERMS					
16. SECURITY CLASSIFICATION OF:			17. LIMITATION OF ABSTRACT <b>Same as Report (SAR)</b>	18. NUMBER OF PAGES <b>354</b>	19a. NAME OF RESPONSIBLE PERSON
a. REPORT <b>unclassified</b>	b. ABSTRACT <b>unclassified</b>	c. THIS PAGE <b>unclassified</b>			

# THE LEAD FREE ELECTRONICS MANHATTAN PROJECT – PHASE I

PRESENTED BY

THE BENCHMARKING AND BEST PRACTICES

CENTER OF EXCELLENCE

Distribution Statement A: Approved for public release; distribution is unlimited.

30 July 2009

Copyright 2009, ACI Technologies, Inc. All Rights Reserved, including rights of the U.S. Government under Contract No. N00014-08-D-0758.

# ***The Lead Free Electronics Manhattan Project – Phase I***

---



For the men and women of the armed forces

who have dedicated their lives to the cause of freedom.





# Foreword

## FROM THE OFFICE OF NAVAL RESEARCH

The Office of Naval Research (ONR) and the Joint Defense Manufacturing Technology Panel sponsored this Lead Free (Pb-Free) Electronics Manhattan Project in response to the very serious challenges that lie ahead for both the Military and Defense Industries to produce reliable hardware given the current climate within the electronics industry.

The cumulative effect of avoiding the issues associated with the transition to Pb-free electronics by the commercial world can be problematic for future Navy and Military war-fighter programs that rely on the performance and reliability of Mission Critical Hardware. The Navy has recognized that a collective endeavor by the most knowledgeable and credible participants in this project would be a first step in coalescing, organizing – and more importantly – identifying current practices in an attempt to separate relevant and factual information from the anecdotal or often misinterpreted data.

I would like to acknowledge the dedication of the professionals involved in this project, and their efforts to bring resolution to this serious issue for the Navy and Department of Defense. It is a testimony of the force that motivates each of them, as they recognize that the quality and safety of the products their respective organization's produce or support, is of paramount importance to all; through their innovation and entrepreneurship, the success of this project will be worthy of its namesake. For this we are all appreciative.

Dr. Joseph P. Lawrence, III  
Director of Transition  
Office of Naval Research

# FROM THE OFFICE OF NAVAL RESEARCH BENCHMARKING AND BEST PRACTICES CENTER OF EXCELLENCE

The ONR ManTech mission, as manifested through the Navy Centers of Excellence, has placed a critical focus on the technologies, processes, and enabling manufacturing capabilities that provide direct benefit to the warfighter in a cooperative environment with industry, academia, and the Navy warfare centers and laboratories. The Pb-Free Electronics Manhattan Project is an example of the collaboration that is possible, when the ramifications of individualized and fragmented attempts to resolve the Pb-free problem, will not effectuate the change that is needed for the mitigation efforts. As part of the mission of the ONR ManTech platform, the Benchmarking and Best Practices Center of Excellence (B2PCOE) was created to facilitate such projects through the dissemination (sharing) of best-in-class practices, processes, methodologies, systems, and best practices technologies.

The B2PCOE is an important conduit in advancing manufacturing technology through public and private sector partnership, technological innovation, technology transfer, competitiveness, the affordability and performance of defense platforms and weapon systems. Competitiveness is a cornerstone of providing affordable, reliable products and services to the Navy; the ONR ManTech platform is still pursuant to that mission. The data and information collected from the Pb-Free Electronics Manhattan Project will advance the status of the best practices for Pb-free mitigation from its incomplete state to one where a foundation can be established for pursuing innovative and cost effective methods of resolving the problem.

The “Manhattan” style approach offers advantages beyond the scope of Pb-free electronics manufacturing. In fact, it will be a basis for modeling future endeavors of a similar nature, where a cooperative approach supersedes the efforts of any one corporate entity. Certain technical subjects are in such early stages of development, that the ability to bridge the disparity between activities, which foster a beneficially competitive environment, and ones which require an accelerated and collaborative effort, will become critical as benchmarking tools for assessing the value of the “Manhattan” approach on project platforms.

Rebecca D. Clayton  
Program Officer  
Office of Naval Research O3T  
Benchmarking and Best Practices Center of Excellence



# Preface

## EXECUTIVE SUMMARY

The objective of the Pb-Free Electronics Manhattan Project – Phase I has been accomplished. Best practices have been captured and documented in two artifacts. The first artifact articulates best practices identified to mitigate the risks associated with Pb-free electronics usage in high-reliability, high-performance aerospace and defense systems. The second artifact captures the “Manhattan Project” approach as a best practice for addressing pervasive issues facing the manufacturing and customer community.

The set of Pb-free electronics best practices contained in this report constitute the current baseline practices as determined by the assembled team of nationally-recognized subject matter expert scientists and engineers. **Current baseline practice** is defined to be a practice that describes the current state-of-the-art as a baseline against which future improvement can be measured. They are provided as guidelines and will change as additional information is accumulated over time and evaluated. Known issues with the current baseline practices and technical gaps are also identified in the report. Phase II of the Pb-Free Electronics Manhattan Project will build upon this current baseline and develop a three-year roadmap for the Phase III research and development required to deal with those issues.

The second deliverable, prepared concurrently by the Navy ManTech’s Benchmarking and Best Practices Center of Excellence (B2PCOE), deals with the process aspect of the “Manhattan Project” serving as a framework to deal with complex, multi-disciplined technical issues. The B2PCOE study captured this best process practice during the execution of Phase I. The process integrated a set of dynamic, highly skilled scientists and engineers, and helped them converge within a real-time, concentrated working environment to synthesize their collective knowledge and experience into a practical set of findings and guidelines. It is has been validated that the paradigm works and can be used to address other problems that exist across industry that are of a similar pervasive nature.

It is the judgment of the team that the use of Pb-free electronics in products whose life-cycle includes operation in and through harsh environments, poses technical risks that can lead to degraded reliability and reduced lifetimes. Quantification of these technical conclusions within valid statistical confidence bounds remains a gap. Further reliability data is needed in order to unite the existing prediction methodologies, and provide acceptable modeling accuracy. The team also concluded that continued “point solution” projects will not adequately address the spectrum of gaps that exist in the current body of knowledge on Pb-free electronics. Therefore, it is strongly recommended that the subsequent phases of the Pb-Free Electronics Manhattan Project be fully implemented to ensure that the risks imposed by Pb-free electronics in high-reliability, high-performance applications (especially in extreme environments) become fully articulated, quantified, and bounded to ensure viable product design, manufacturing, test, delivery and sustainment at an affordable cost.

## **ACKNOWLEDGEMENTS**

The Pb-Free Electronics Manhattan Project team wishes to acknowledge the U.S. Navy Office of Naval Research (ONR), the ONR Office of Transition and its Manufacturing Technology (ManTech) Directorate, and the Navy ManTech Benchmarking and Best Practices Center of Excellence (B2PCOE) for their foresight in funding the Phase I effort. The team also wishes to acknowledge ACI Technologies for providing the appropriate facilities and process leadership in the development of the Phase I deliverables. Also, a special note of gratitude is extended to the invited guest speakers and other “life-line” subject matter experts that provided support to the project team.

Finally, the team leadership would like to acknowledge the dedicated scientists and engineers who assiduously worked together in an integrated team environment to produce this deliverable.

## PARTICIPANTS

### Program Management Team

Function	Point of Contact	Company
U.S. Navy ManTech Director	John Carney	Office of Naval Research
Program Officer	Rebecca Clayton	Office of Naval Research
B2P Director	Mike Frederickson	ACI Technologies, Inc.
Project Manager	Carmine Meola	ACI Technologies, Inc.
B2P Lead	Michael Barger	ACI Technologies, Inc.
Technical Lead	Gerald Aschoff	Boeing
Technical Lead	Ed Morris	Lockheed Martin
Moderator	Dr. Richard Reilly	Howe School of Technical Management Stevens Institute of Technology

### Subject Matter Experts

Function	Point of Contact	Company
Subject Matter Expert (SME)	Dr. Peter Borgesen	Binghamton University
SME	Lloyd Condra	Boeing
SME	Dr. Carol Handwerker	Purdue University
SME	Dr. Craig Hillman	DfR Solutions
SME	David Hillman	Rockwell Collins
SME	David Humphrey	Honeywell
SME	David Locker	AMRDEC
SME	Dr. Stephan Meschter	BAE Systems
SME	Dr. Michael Osterman	University of Maryland - CALCE
SME	David Pinsky	Raytheon

**Preface**

---

---

Function	Point of Contact	Company
SME	Dr. Anthony Rafanelli	Raytheon
SME	Dr. Polina Snugovsky	Celestica
SME	Fred Verdi	ACI Technologies, Inc.
SME	Dr. Paul Vianco	Sandia National Labs
SME	Maureen Williams	NIST
SME	Dr. Thomas Woodrow	Boeing
SME	Linda Woody	Lockheed Martin



*The Lead Free Electronics Manhattan Project Team*

## **Guest Speakers and “Life-line” Supporters**

<b>Point of Contact</b>	<b>Company</b>
Michael Carano	OMG Group, Electronic Chemicals
Patrick Clavette	United Technologies
Jean-Paul Clech	EPSI Inc.
Dr. Abhijit Das Gupta	University of Maryland - CALCE
Gordon Davy	Northrop Grumman (Retired)
Joel Heebink	Honeywell
Matthew Kelly	IBM
Dr. Pradeep Lall	Auburn University - CAVE <sup>3</sup>
Jin Lang	EMC
Dr. Henning Leidecker	NASA Goddard
Kamran Mohajer	Cisco Systems, Inc.
Todd Mulder	Honeywell
Gregory Munie	Kester Solders
Richard Parker	Delphi Corporation
Joseph Smetana	Alcatel Lucent
Dr. Jeffrey Suhling	Auburn University - CAVE <sup>3</sup>

# Table of Contents

I	Foreword .....	i
II	Preface .....	iii
	Executive Summary .....	iii
	Acknowledgements.....	iv
	Participants .....	v
1.	Introduction.....	1
	1.1 The Current Electronics Business Environment.....	1
	1.2 Pb-Free Electronics Manhattan Project.....	2
	1.3 Pb-Free Best Practice Deliverable.....	3
2.	Pb-Free Overview.....	6
	2.1 Overview of the Current State.....	6
	2.2 Major Risks Associated with the Use of Pb-Free Electronics .....	7
	2.3 Relevance to Warfighter .....	8
	2.4 Remediation of Risks.....	9
	2.5 Pb-Free Electronics Cultural Issues .....	12
3.	Design.....	14
	3.1 Introduction.....	14
	3.2 Requirements .....	25
	3.3 Hardware Design.....	61
	3.4 Design Verification/Validation .....	83
	3.5 Tin Whisker Risk Assessment.....	104
	3.6 Reliability Analysis.....	109
	3.7 Safety and Non-Safety Systems Certification .....	110
	3.8 Manufacturing Handoff .....	111
	3.9 Sustainment Handoff.....	112
4.	Manufacturing.....	114
	4.1 Introduction.....	114
	4.2 Design for Manufacturing.....	116
	4.3 Staging .....	122
	4.4 Solder Paste Deposition .....	123
	4.5 Component Placement.....	123
	4.6 Solder Metallurgy - Solder Joint Formation .....	124
	4.7 Solder Processes .....	143
	4.8 Depaneling/Routing.....	152

4.9	Cleaning .....	153
4.10	Underfill Process .....	154
4.11	Inspection Processes .....	155
4.12	Rework .....	158
4.13	Conformal Coating .....	160
4.14	Test .....	162
4.15	Pack and Ship .....	163
5.	Sustainment .....	165
5.1	Introduction. ....	165
5.2	Configuration Management .....	167
5.3	Logistics .....	171
5.4	Repair .....	173
6.	Testing .....	182
6.1	Introduction .....	182
6.2	Testing for Materials Properties and Product Manufacturability .....	183
6.3	Material Testing for Computational Modeling .....	194
6.4	Circuit Card Assembly Testing .....	205
7.	Reliability .....	213
7.1	Introduction .....	213
7.2	Failure Sources .....	219
8.	Conclusions .....	243
9.	Recommendations .....	250
III	Appendix A – Supplemental Information .....	256
	Chapter 2 .....	256
	Chapter 4 .....	257
	Chapter 6 .....	258
	Chapter 7 .....	278
IV	Appendix B – Case Study .....	281
V	Appendix C – Biographies .....	298
VI	References .....	309
VII	Index .....	319

“There are two possible outcomes: If the result confirms the hypothesis,  
then you’ve made a measurement. If the result is contrary to the hypothesis,  
then you’ve made a discovery.”

—*Enrico Fermi (1901-1954)*



Trinity Site Monument • New Mexico, USA



# 1. Introduction

## 1.1 THE CURRENT ELECTRONICS BUSINESS ENVIRONMENT

The worldwide electronics supply industry is adopting lead (Pb) free materials and processes in their manufactured and assembled electronics products. Ultimately, these Pb-free electronic assemblies are being introduced into the inventories of Original Equipment Manufacturers (OEMs) who must make a determination as to whether to use them, reject them, or rework them. This decision process is driven by the fact that the use of Pb-free electronics poses a potential product risk and could compromise end item product reliability when subjected to harsh environments and long service life-times.

Although the European Union (EU) legislation was the initial reason for suppliers to transition to Pb-free electronics, many have been transitioning for a myriad of other reasons such as establishing a competitive advantage in the marketplace.

Aerospace and Defense OEMs are at risk because they are unable to control the global electronics supply chain because their collective demand is low compared to that of commercial manufacturers. Establishing control over this supply chain by high-reliability users such as the Department of Defense (DoD) and the commercial airline industry is futile. Over 50% of the electronics manufacturing today is conducted off-shore to the U.S.A., and the collective demand by all of the military electronics users represents less than 1% of the total world-wide market. Consequently, it is inevitable that they will unknowingly receive Pb-free components in place of SnPb-based electronics, regardless of what was ordered.

Factors which exacerbate this risk are:

- A lack of standardization as to what type of data and the level of data that should be provided by the suppliers when they deliver materials or parts.
- A lack of material characterization data required to establish confidence in part usage and uncertainty regarding the test protocols currently established to yield confidence data. The current test standards and protocols (e.g., temperature cycling and dwell times, mechanical shock and vibration tests, etc.) have evolved and are interpreted based upon 50 plus years of experience using eutectic Pb-based solder alloys, and may not provide the appropriate stress test conditions for Pb-free based solder alloys. Hence, currently there is no standard test protocol available to qualify Pb-free electronic products, other than the fallback position of using existing standards which are based on Pb.
- A lack of standardized manufacturing, assembly, rework and repair processes due to a dearth of information and standards on how to sustain Pb-free products.

## 1. Introduction

---

All of these factors contribute to an Aerospace and Defense (A&D) OEM dilemma where there is little to no contractual guidance to help steer the use of Pb-free electronics materials and processes. Yet the supply chain that OEMs depend upon continues to transition and propagate Pb-free usage.

Consequently, A&D OEMs are ultimately being forced to use Pb-free electronics or implement costly processes to ensure their denial. Either option has an impact on product acquisition and Total Ownership Cost (TOC). Denial of Pb-free electronics will restrict the use of commercial off the shelf (COTS) products and increase platform cost. Admission of Pb-free electronics into the build of material will require re-qualification of the manufacturing processes and products, further increasing platform cost. Either option increases the end-item's TOC. Sustainment of these platforms necessitates greater attention to manage and control electronics inventories, while preparing for the use of specialized rework and repair processes to maintain a "Pb-only" baseline, as well as a Pb-based and Pb-free component mix.

### 1.2 PB-FREE ELECTRONICS MANHATTAN PROJECT

The Pb-Free Electronics Manhattan Project was motivated by the desire to mitigate the increasing risk associated with the proliferation and use of commercial Pb-free electronics in OEM products. The concept for a Pb-Free Electronics Manhattan Project was initialized, formulated, and "socialized" across industry and the customer community in order to obtain sponsorship and consensus. The project was envisioned as a single, fully-funded team of nationally recognized scientists and engineers working cooperatively over a three-year period, focused on addressing the use of Pb-free electronics in A&D products.

The project has been segmented into three phases with the primary funding (estimated to be \$60M) expected in Phase III. Phase I was planned to establish the baseline in terms of documenting current practices used across industry, and identifying the issues and gaps associated with those practices. Phase II plans to articulate the roadmap which identifies future work required to mitigate those issues and close the gaps in order to reach an acceptable risk level. These two phases will form the basis for the expanded scope of Phase III of the Manhattan Project, which will focus on the conduct of specific tasks that address these identified gaps. Phases I and II were planned as distinct, separate two-week projects conducted in a single geographical location, such as a national lab, using a skilled set of recognized scientists and engineers.

The deliverable associated with Phase I is the main subject of this document. The Manhattan Project is unique because it represents the best in class from industry, academia, and government working cooperatively to resolve a pervasive risk facing A&D OEM product suppliers.

1.3 PB-FREE BEST PRACTICE DELIVERABLE

The Phase I deliverable articulates current state-of-the-art best practices as a baseline against which future improvements will be enacted. The body of this report has been organized and structured to flow as a typical product life cycle, initiating with requirements and concluding with end of life as shown in Figure 1.1, Product Life Cycle Diagram.

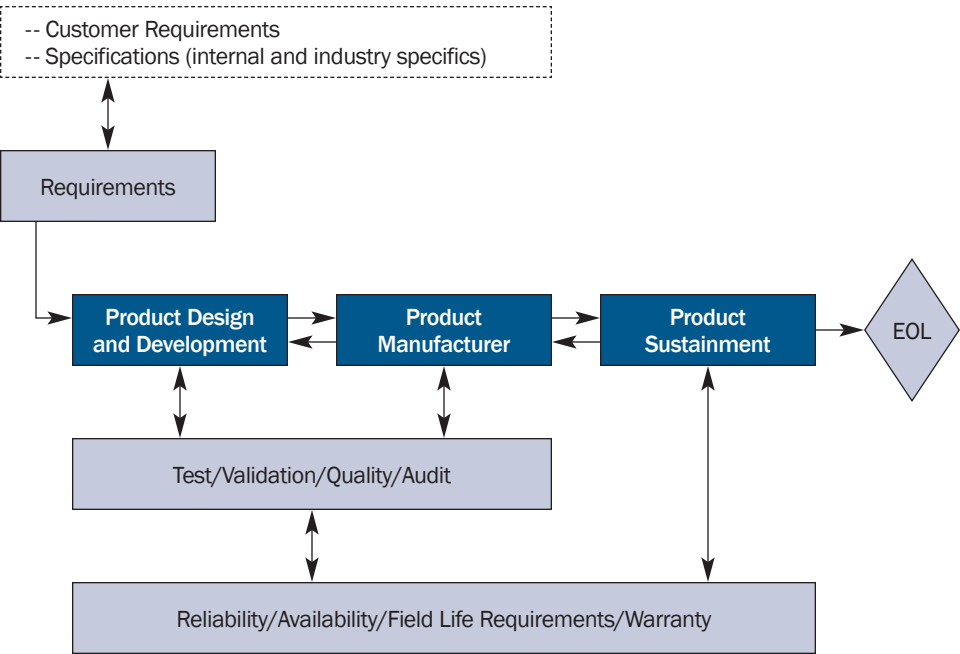


Figure 1.1 Product Life Cycle Diagram: Pb-free usage impacts all phase of the life cycle of a product.

## 1. Introduction

---

This report captures the impact of Pb-free electronics for each block illustrated in the product life cycle. Figure 1.1 also illustrates that Reliability and Test are common elements that are interwoven as part of the supporting infrastructure used throughout the product life cycle. The document structure follows this product life cycle and highlights those elements, which are impacted by the use of Pb-free materials. Each section in the document identifies the current set of baseline practices, issues and gaps, and conclusions and recommendations associated with their use. This is then followed by an overall synopsis of the conclusions and recommendations extracted from the body of the report. A summary level outline for the document is as follows:

- Preface
- Introduction
- Pb-Free Overview
- Design
- Manufacturing
- Sustainment
- Testing
- Reliability
- Conclusions
- Recommendations
- Appendices

“Give me a lever long enough and a fulcrum on which to place it,  
and I shall move the world.”

—*Archimedes (circa 287-212 BC)*



Temple of Apollo • Corinth, Greece

# 2. Pb-Free Overview

## 2.1 OVERVIEW OF THE CURRENT STATE

The restriction and elimination of lead (Pb) in electronics products was initiated by legislation enacted within the European Union [i.e., Restriction of Hazardous Substances (RoHS) in Electrical and Electronic Equipment; Waste from Electrical and Electronic Equipment (WEEE)] and Pacific-Rim geographical regions (circa 2006). Many non-U.S. countries have followed suit in order to restrict the disposal of electronic products containing Pb within their boundaries. The U.S. does not have existing federal legislation, but several states have adopted laws restricting Pb content in the manufacturing and disposal of electronic equipment. To date, Aerospace and Defense OEMs are exempt from this legislation.

The general definition of Pb-free is depicted in Europe and in the U.S. as packages that contain solder and other materials that have a maximum of 0.1% Pb (percent by weight). Legislation to restrict Pb content in electronics led to a technology shift in the global electronics supply chain. For a myriad of reasons including increasing their capture of market share, suppliers have been transitioning to using Pb-free processes and supplying Pb-free materials. This transition or shift in the supplier baseline has undermined the fundamental process of how electronics assemblies are built and has led to a technology disruption and potential risk at the A&D OEM product level.

A&D OEMs had established their product designs and builds predicated upon the use of a stable SnPb baseline. As suppliers have changed to a Pb-free baseline, OEMs have been driven to increase the awareness of Pb-free use, while understanding its impact upon their product performance and establishing risk mitigation processes for its use; thus creating a pervasive issue. Exacerbating this issue is the fact that a single “drop-in” replacement for the legacy SnPb baseline does not exist. In fact, the opposite situation exists since there are a myriad of Pb-free materials which are being supplied and used as replacements across the worldwide supplier community. Furthermore, the Pb-free materials demand by commercial consumers has contributed to their proliferation as consumer and commercial electronics OEMs have determined that Pb-free materials were adequate for their markets.

The primary issue associated with the use of Pb-free materials is that the reliability of A&D products built using this technology in typically “harsh environments” and requiring long product lives, is un-quantified. Pb-free does not have the legacy of over 50 years of supporting performance data, as in the case for SnPb. A&D product lives are often measured in decades compared to the typical commercial product life, which is measured over a few years. These factors contribute to the risk associated with Pb-free electronics, and the uncertainty of how to adequately address them within current required product life cycles. Engineers using SnPb electronics have evolved to be good rule followers. However, in this new paradigm, Pb-free electronics will require engineers to create new rules-of-thumb.

The customer base has a general awareness of Pb-free electronics use, but reliance upon performance-based procurements has shifted the burden of awareness and product risk mitigation to the A&D OEMs. Unfortunately, without a uniform approach and existing standards to guide the OEMs, a current state exists where A&D OEMs can deliver an assortment of mixed SnPb and Pb-free, and/or wholly Pb-free products based upon their own preferred approach. The end result will be a set of products that the customer must ultimately maintain, which to some extent contain product pedigrees that are unknown and whose build of materials vary widely. This situation greatly impacts product sustainability and leads to a high TOC and a logistical quagmire. Extrapolation of this situation leads to a state of unrestrained cost growth.

## 2.2 MAJOR RISKS ASSOCIATED WITH THE USE OF PB-FREE ELECTRONICS

The major risks confronting products which introduce Pb-free electronics into their build of material may be divided into two categories: product reliability and product sustainment. Product reliability encompasses those risks which impact the reliability of the product required to operate as desired, in the defined environmental applications outlined in its contractual service life. The primary product reliability risks related to Pb-free electronics is the premature failure of the solder joint interface and functional failures caused by tin whiskers. Both reliability risks are addressed in detail in this document. Product sustainment includes those risks which impact the projected lifetime of the product to include its availability and total ownership costs. These general risks may be further subdivided into the following risk factors.

2. Pb-Free Overview

Product Reliability Risk Factors	Product Sustainment Risk Factors
Build of Material:	Build of Material:
COTS/GOTS	Configuration Management
PWB Design and Finishes	Repair Level and Instructions
Solder Attachments and Finishes	Inventory Management
Component Finishes to include Sn Whisker Issues	Availability of Correct Parts and Solders
Mechanical Parts and Finishes to include Sn Whiskers	Training of Depot Personnel
Reliability Demonstration (Test or Analysis)	Documentation (e.g., Technical Baseline)
Product Manufacturing Processes to include Rework and Test	

Table 2.1 Pb-free electronics risk factors. Use of Pb-free electronics poses risk to product reliability and sustainability; shown are those risk factors which must be addressed in the life cycle.

2.3 RELEVANCE TO THE WARFIGHTER

The warfighters that defend the United States expect and deserve weapon systems and equipment that have superior technical performance and unquestionable reliability. This demand is exacerbated by the unique applications required in urban warfare against terrorists imbedded in civilian populations. This highlights the criticality that the weapons and equipment function correctly, and without failures. To minimize collateral damage, the numbers of weapons used against an urban target have been reduced, further mandating that each weapon perform flawlessly. Product failures in the midst of a battle can have catastrophic results, jeopardizing the outcome of a conflict and exposing our warfighters to needless injury, and even loss of life.

The systems must also be sustainable in the field and be quickly, easily and cost effectively repaired when needed to bring a damaged system back on line.

Given the high reliance on electronics in weapon systems and military equipment, it is paramount that the issues and technical risks from Pb-free electronics, highlighted in Figure 2.1, be fully understood and mitigated.



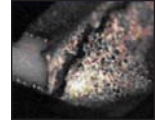
### Pb-Free Electronics – So What?

Pb inhibits the growth of “tin whiskers”

- Electrically conductive
- Can metal vapor arc



Pb-Free Solder Joint  
Electromagnetic Relay

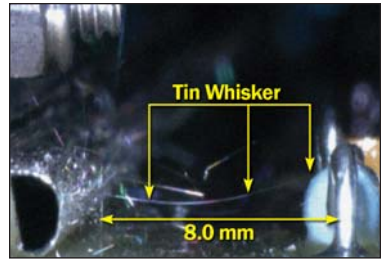


Pb-free solders

- Less reliable when subject to high shock and vibration
- Higher melting temperatures
- Incompatibilities with SnPb solder
- Difficult to repair assemblies

Configuration control nightmare

Photo Source: NASA Space Shuttle Program



**Figure 2.1** Sample of Pb-free electronics issues. Focused research and development is required to maintain unquestioned reliability when using Pb-free electronics in warfighter weapons systems and equipment.

## 2.4 REMEDIATION OF RISKS

The transition to Pb-free materials by electronics suppliers initiated a movement among the OEMs to recognize it as a pervasive issue and acknowledge that a collective approach was necessary to manage and mitigate its risk. After reviewing the situation, it was concluded that the risk remediation solution set was non-competitive since it involved the synthesis of numerous data sources. In addition, single company investment strategies to achieve this state were deemed to be cost prohibitive. Hence, early on in the awareness and risk mitigation approach to Pb-free electronics, the industry sought to develop inclusive collaborations to address and manage the risk. The ONR had pro-actively funded several ManTech projects that lead to the publication of “Lead Free Manufacturing for Navy Systems,” among other efforts. Other collaborations across industry, ONR, DoD, NASA, and AIA, resulted in the Pb-free Electronics in Aerospace Project (LEAP) and the cooperative Government/Industry Executive Pb-Free Integrated Process Team (ELF IPT) projects. LEAP focused on the development of standards and their publication. The ELF IPT focused on awareness, training, and policy.

The Electronics Manufacturing Productivity Facility (EMPF), with funding from the ONR, had initiated several projects to determine what affect lead free soldering technologies would have on aerospace and military applications. The EMPF performed a number of manufacturing infrastructure audits, and in cooperation with the Industrial Advisory Board (IAB) members, had built and tested functionally

## 2. Pb-Free Overview

---

deliverable hardware manufactured with lead free solders. The study – conducted by the EMPF, member companies of the IAB, Joint Council on Aging Aircraft (JCAA), Joint Council on Pollution Prevention (JC-PP), and CALCE – was a collaboration of experimental efforts to observe the effects of Pb-free on various test vehicles designed to simulate hardware typically used in Navy systems. The results from some of those studies are referenced in the body of this report. In addition to the Navy endeavors in the area of Pb-free mitigation, cooperative efforts from organizations such as iNEMI, NIST, CALCE, and IPC had individually and collectively performed research and development tasks on lead free solders.

Knowing that the reliability of Pb-free parts in military systems was a significant issue, the Executive Lead Free Integrated Process Team (ELF IPT), composed of representatives from industry and government, cooperated to advise the DoD (Department of Defense) on critical issues surrounding Pb-free electronics. In turn, the DoD commissioned the ELF IPT to advise on a joint DoD response in order to minimize any disruption of the supply or reliability of electronics, particularly COTS (commercial-off-the-shelf) components and sub-assemblies. The web site representing the efforts of the DoD and the ELF IPT ([leadfreedod.com](http://leadfreedod.com)) continues to be maintained by the EMPF. The Aerospace Industries Association (AIA) has also contributed to the movement with its Lead-Free Aerospace Electronics Working Group (LEAP), beginning in 2004. Its purpose was to “develop and implement actionable deliverable items that enable the aerospace industry to accommodate the global transition to lead-free electronics.”

From these activities, certified standards were generated and functional avionics were manufactured with lead free solder alloys and finishes by DoD supplier facilities such as the EMPF, operated by ACI Technologies. The demonstration vehicle(s) and target programs were the F/A-18 and the AEGIS Integrated Weapons Systems. Electronics manufacturing processes, required to produce qualified functional Navy electronic hardware which meets IPC J-STD-001D Class 3 and IPC-A-610 Class 3 specifications, were documented. Both the Lead-Free Soldering Standard (ACI-081906) and the Lead-Free Manufacturing Guidelines (ManTech Lead-Free Manufacturing Guidelines, 8/18/2006) have been published and are available for use in manufacturing, reworking, and repairing lead free electronics for Navy applications.

While the efforts highlighted above were desperately needed to better understand the implications of lead free solder, they only scratch the surface from the perspective of the needs of the DoD/ aerospace reliability engineering community. For example, the Aviation and Missile Research, Development and Engineering Center (US Army Aviation and Missile Command), or AMRDEC, is faced with the problem of reliability over time, as missiles are stored for years. Stockpile Reliability Programs (SRP) defined and carried out by the reliability experts at AMRDEC have been instrumental in maintaining the necessary level of stockpile reliability at an affordable cost. But now, with the transition to lead free connections, a whole new set of challenges arise to maintaining that stockpile. The AMRDEC leadership has anticipated the issues and has worked with others in the U.S. government facing similar challenges, such as the Department of Energy (DOE). Cooperative efforts under the banner of the Technical Coordinating Group for Predictive Materials Aging and Reliability (TCG XIV)

were begun to “develop a toolset of computational models that are able to quantitatively predict materials aging processes for improving the long-term reliability of weapons systems, sub-assemblies, and/or components.” To date, AMRDEC has managed related SBIR efforts under several projects to assess the reliability of lead free solder.

The EMPF, through Navy ManTech efforts, has endeavored to provide technical and project management to the various aforementioned organizations and consortia which have contributed significantly in researching the areas of Pb-free manufacturing, technology, process development, standards development, reliability, and tin whisker mitigation. As these groups continued to work together over several years, an evolutionary restructuring was considered as a means of uniting the groups under the current Pb-free Electronics Risk Management (PERM) Consortium structure. The shift to the more robust PERM Consortium framework was driven by a clear sense that although both the LEAP and ELF IPT groups were doing good work to deal with the Pb-free electronics issues, our overall national strategic response was inadequate and poorly coordinated. The PERM Consortium concept was briefed to the Aerospace Industries Association’s Technical Operations Council (AIA TOC) in December, 2008 and was formally endorsed in January, 2009.

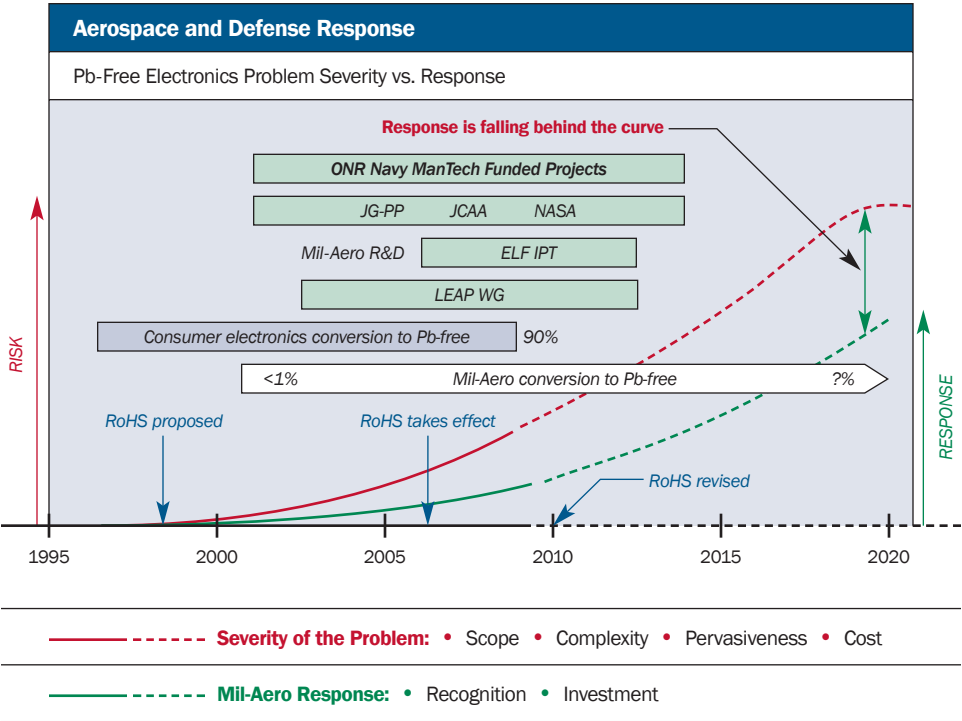


Figure 2.2 A&D response to Pb-free electronics. Good progress was made through 2008, but a more robust national strategic response was needed to deal with the risks posed by Pb-free electronics.

## 2. Pb-Free Overview

---

The PERM Consortium strategic management framework represents an organizational construct that integrates the myriad of Pb-free electronics activities (existing and proposed) into organized subsets of related activities (see Appendix A, Chapter 2 for PERM organizational chart). These activities include the industry, academia, consortium, and government sponsored projects which become united under the PERM structure into a single organizational architecture.

The Pb-free Electronics Research Manhattan Project was planned as a multi-phased R&D project. Phases I and II are currently funded by the Department of Defense. This report is a result of the Phase I effort and identifies the current baseline practices in use to deal with Pb-free electronics. The Phase II effort, scheduled for August, 2009, will develop a three-year roadmap of the time-phased R&D projects recommended for risk reduction scheduled for execution during Phase III. The roadmap will further articulate the gaps that exist in relation to the risks associated with the use of Pb-free electronics, and will recommend the necessary R&D tasks required to fill those gaps. The Phase II roadmap will present an integrated approach to an insidious and pervasive problem facing the aerospace and defense community today. Government funding is needed to initiate and execute the Phase III effort.

### 2.5 PB-FREE ELECTRONICS CULTURAL ISSUES

Adding to the Pb-free electronics challenges, are cultural issues which are as complex as the technical issues. Due to the cross-cutting and multi-faceted technical issues, the first cultural issue encountered is that “this is everyone’s problem, therefore it’s no one’s problem.” As a result, finger-pointing ensues and mitigation time is lost. Impacted organizations attempt to identify who should be responsible for dealing with the multiple Pb-free electronics issues, including who should provide requisite funding. This approach is not remedial or helpful.

Other fundamental Pb-free electronics cultural issues are embodied in the captured actual quotes of leaders in both government and industry:

*“I have more important, immediate problems.”*

*“I cannot obtain funding for a research project for which there is no clear solution, no definitive schedule, and no grasp of the total funds required.”*

*“Show me the recent evidence that this is a problem that merits my attention.”*

versus

*“We cannot share this with anyone.”*

Each of these perspectives is an additional excuse for inaction, perhaps hoping that the problem will just go away. Regrettably, doing nothing is not deemed to be the right answer.

“Do not worry about your difficulties in Mathematics.

I can assure you mine are still greater.”

—Albert Einstein (1879-1955)

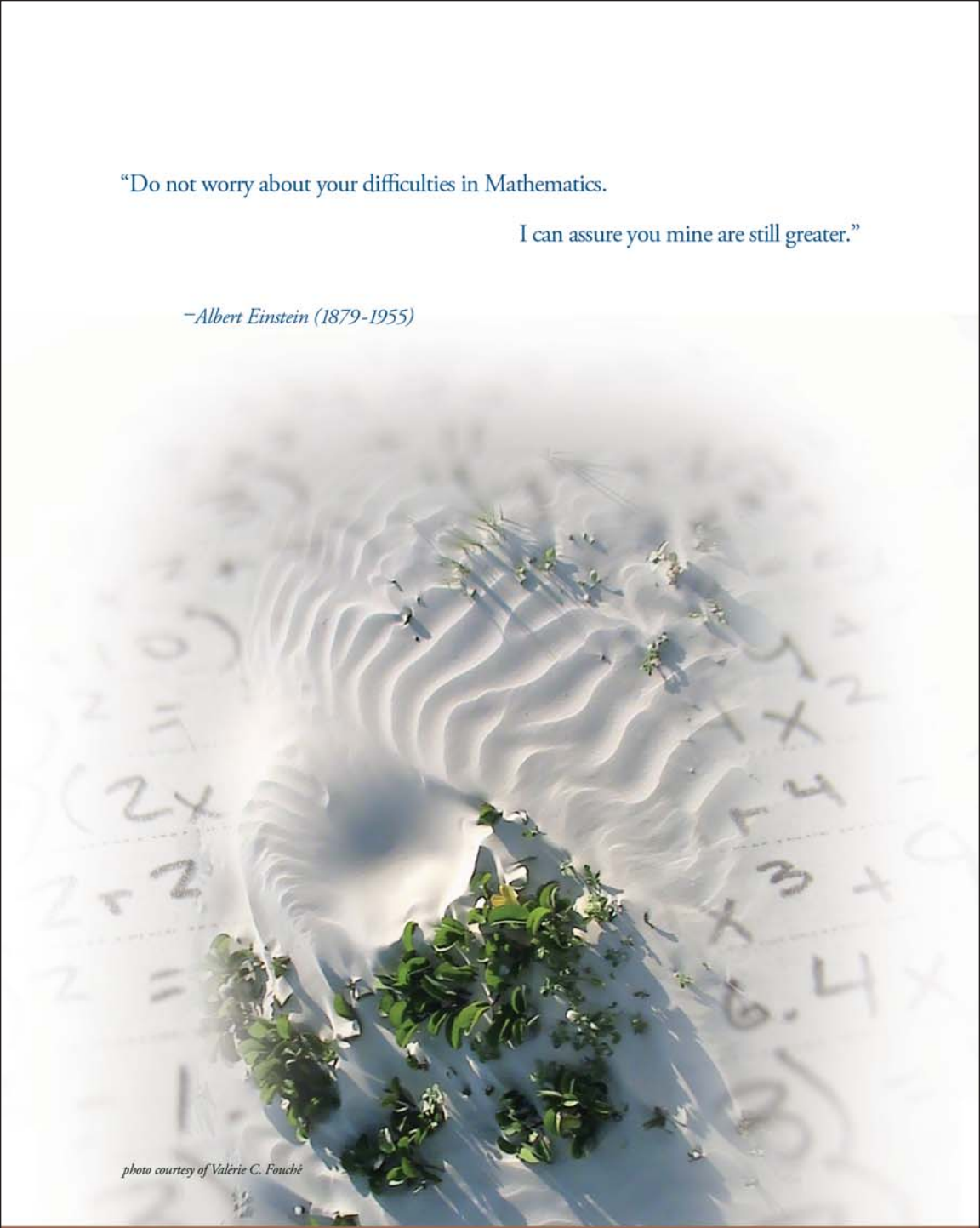
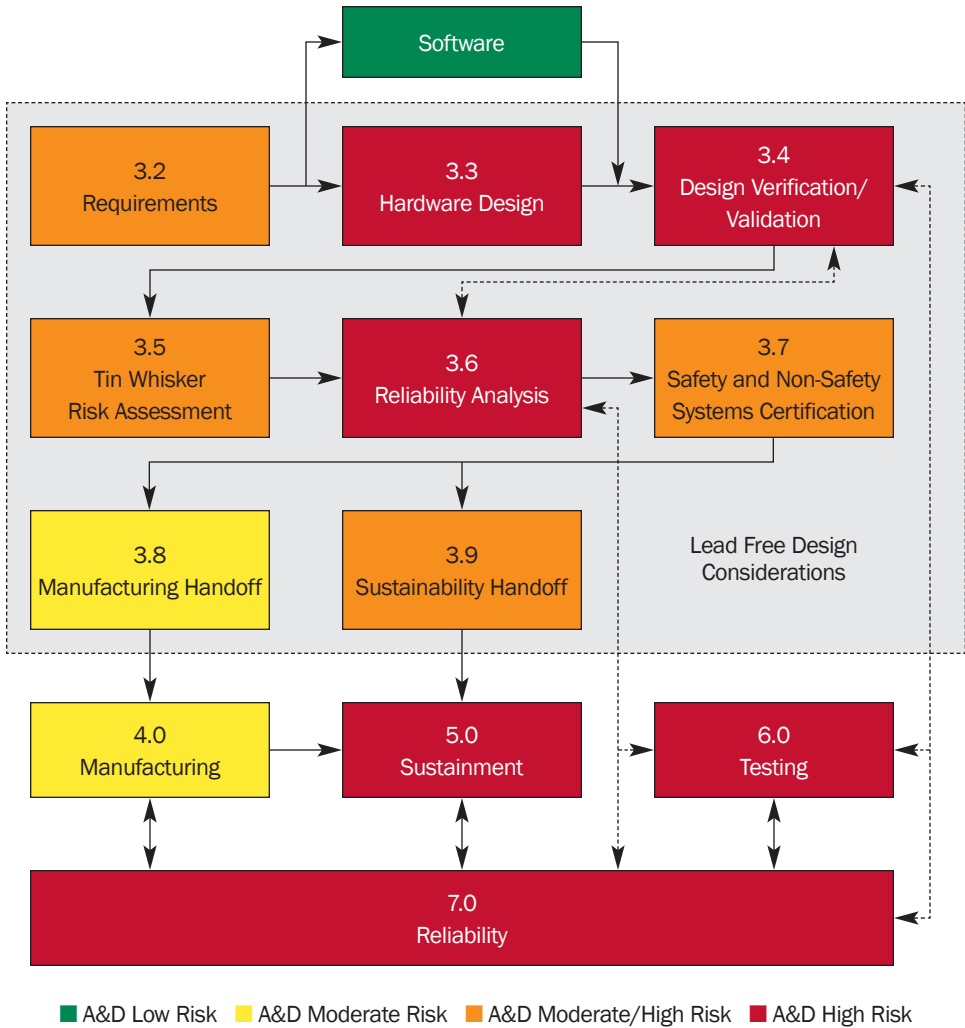
A surreal landscape featuring sand dunes with ripples. The background is a light, hazy sky. The sand dunes are covered with faint, handwritten mathematical equations and numbers, including  $2 =$ ,  $(2 \times$ ,  $2 + 2$ ,  $2 =$ ,  $1.$ ,  $1 \times 2$ ,  $+ 4$ ,  $\times 3 +$ ,  $6.4 \times$ , and  $8)$ . Several small, green, leafy plants with white flowers are scattered across the dunes, particularly concentrated in the foreground and middle ground. The overall scene is dreamlike and artistic.

photo courtesy of Valérie C. Fouché

# 3. Design

## 3.1 INTRODUCTION

The product development cycle as outlined in Figure 3.1, shows that the inclusion and ramifications of Pb-free materials begins at the platform requirements phase and propagates through to product sustainment. While eutectic and near-eutectic SnPb alloys have long been the benchmark for electronic assembly, Pb-free solder and Pb-free surface finishes present challenges in design and qualification test development for A&D equipment. Under some accelerated thermal cycling conditions, consumer Pb-free assemblies have been reported to have good reliability with respect to SnPb assemblies. However, Pb-free consumer hand held devices have been found to have lower reliability in drop-shock testing than the SnPb counterparts. Unfortunately, little testing has been done for the full spectrum of A&D environments such as extended storage, thermal cycling, vibration, shock, humidity, and corrosion, or some combination of these tests. As is outlined in Table 3.1, Pb-free is not as consistently reliable as SnPb, and can introduce additional failure modes not normally associated with SnPb assemblies. As a result of not having a drop-in replacement for SnPb, the design details at every level need to be evaluated. While high-volume design and manufacturing of Pb-free assemblies have been developed over the last 10 years, A&D designs that utilize Pb-free solder in severe or complex operating environments are only beginning to be done. It is well known that the increased processing temperatures of Pb-free solders have caused the manufacturing process windows to tighten significantly. As a result of this change, designs for consumer products have adapted to meet the demands of high volume manufacturing, while A&D designs will have had to settle for lower yields in a manufacturing environment where a high mix of products at low volumes is typical. Additionally, A&D designs must also accommodate long term reliability and sustainability requirements that are not usually mandatory for consumer products.



**Figure 3.1. Design in Product Development Cycle.** Note the risk color coding is based on having both Pb-free finished parts and Pb-free soldered assemblies.

3. Design

Assembly Solder			
Factor Under Consideration <sup>1</sup>	SnPb	Pb-Free Tin Finish and Solder (SAC)	Certainty
SAC Solder Fatigue			
Storage (followed by thermal cycle, vibration and shock)			
Long Term 125 °C	Current Baseline Practice	Worse	High
Long Term -40 to -55 °C	Current Baseline Practice	Worse	High
Thermal Cycling Testing			
Low Stress 0-100 °C	Current Baseline Practice	Better	High
High Stress -55 to +125 °C	Current Baseline Practice	Somewhat Worse	High
Service Life Model	Current Baseline Practice	SAC305 and 387 models exist but lack diverse long term data.	High
Mechanical Dynamic			
Vibration	Current Baseline Practice	Worse	High
Shock	Current Baseline Practice	Worse	High
Handling/Drop Impact	Current Baseline Practice	Worse	High
Service Life Model	Current Baseline Practice	Unknown: SAC 305 beginning to be formulated.	High



Assembly Solder			
Factor Under Consideration <sup>1</sup>	SnPb	Pb-Free Tin Finish and Solder (SAC)	Certainty
Combined Environment			
Thermal/Vibe/Shock	Service Experience	Worse	Medium
Service Life Model	Poor	Unknown	High
Other Failure Modes			
Tin Whisker Risk	Very Low	New Mode: High Risk	High
Tin Pest Risk (Solder disintegration or strength degradation)	Very Low	New Mode: High Risk. <sup>2</sup> Inhibited by Pb, Bi, and Sb additions. Made worse with several factors including reactor radiation exposure. <sup>3</sup>	Low-Medium
PCB Considerations			
PCB Design	Current Baseline Practice	Increased Risk	High
PCB Surface Finish	Current Baseline Practice	ENIG Increased Risk in manufacturing assembly and reliability.	High
PCB Laminate Fracture Under Pads	Very Low	New Mode: High Risk	High
PCB Copper Dissolution	Very Low	New Mode: Increased Risk	High
PCB Surface Copper Trace Fracture	Very Low	New Mode: Increased Risk	High

3. Design

Factor Under Consideration <sup>1</sup>	Assembly Solder		Certainty
	SnPb	Pb-Free Tin Finish and Solder (SAC)	
PCB PTH Reliability	Current Baseline Practice	Increased Risk	High
PCB CAF	Current Baseline Practice	Increased Risk	High

■ Low Risk   ■ Moderate Risk   ■ High Risk   ■ Unknown

Table 3.1 SAC Solder fatigue, Pb-free tin failure modes and printed circuit board (PCB) failure modes.

<sup>1</sup>SAC = Pb-free tin/silver/copper alloy; PCB = printed circuit board; PTH = plated through hole; CAF = conductive anodic filament; SnPb = SnPb eutectic solder alloy

<sup>2</sup>Applications requiring months or years of continuous cold storage such as space, arctic or antarctic environments.

<sup>3</sup>See GEIA-HB-0005-2 Section 5.2 and references in Becker [1].

3.1.1 Key Design Considerations

The designer utilizes critical information to assess the various constituents that will ultimately comprise the final design. Customer requirements, reliability data, test methods, reliability model maturity, failure mode types, manufacturing processes, and sustainment are all factors that will be considered in the construction of a Pb-free design.

Often the first decision that a designer needs to make is what solder or solders to select. As is shown in Figure 3.2, the Pb-free solder microstructure (SAC) differs significantly from SnPb. Since the microstructure controls the properties, the methods and parameters implemented in SnPb mechanical testing and analysis need to be reconsidered in terms of adapting for new Pb-free material properties and failure modes [2] [3]. The next stage is to determine which parts are acceptable for the new design, and which are subsequently added as part of a newly created bill of material. As the printed circuit board (PCB) and circuit card assembly (CCA) designs are completed, concurrent electrical, mechanical and testing analysis are being completed to verify and validate the design, as well as the design process. Some of the high level design considerations are summarized in Table 3.2.

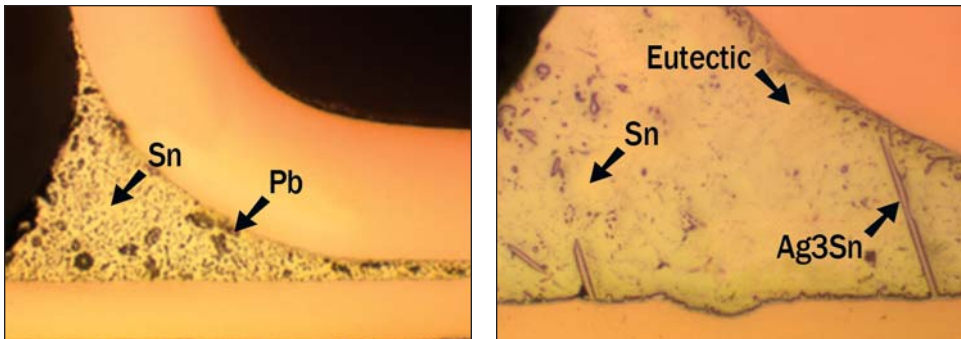


Figure 3.2 An example of dramatic differences in microstructure between SnPb (left) and Pb-free SAC (tin-silver-copper alloy) (right) solders. Photo courtesy the Celestica Company.

Issue	Considerations
<b>Solder</b>	
Many alloys to chose from	Eutectic alloys are preferred. Alloy defines the manufacturing process temperature. Alloy defines rework and repair processes.
Complexity of the alloy (constituents)	Sensitivity of final solder properties and the variation in final microstructure to weight percent variation of the constituents.
Material properties	Maturity, acceptance and validation. Usefulness for solder joint size scale modeling.
Fatigue models	Maturity, acceptance and validation.
Accelerated testing	Maturity, acceptance and validation of thermal cycling, vibration, shock, combined TC/Vibe/Shock, humidity, corrosion, etc.
Manufacturing processing temperature	A 5 or 10 °C change in soldering temperature is significant for PCB materials and copper dissolution.
Compatibility with SnPb	Sustainment strategy.
Mixing with other Pb-free alloys	Manufacturing and sustainment concerns.
Tin whisker risk	Tin whisker growth characteristics.

### 3. Design

---

---

Issue	Considerations
Tin pest	Tin pest resistance.
Copper dissolution	Tendency to dissolve copper PCB terminations.
Field experience and field failure data	Experience with alloy and parts in similar applications and environments.
Parts	
Temperature capability	MSL level and maximum solder processing temperature.
Internal construction materials	Reliability of internal Pb-free solders and tin whisker risk often difficult to determine with COTS parts.
External finish and lead material	Tin whisker risk.
Molding compound	Part CTE can be reduced when Pb-free compatible molding compounds are used.
Reliability data	Has part reliability changed with Pb-free processing temperatures and under the Pb-free solder termination loads?
Compatibility with SnPb solder	Are the part finishes or balls reliable when processed with SnPb solder?
PCB	
Laminate selection	Higher cost laminates are available to meet higher reflow temperatures. Considerable reliability variability exists amongst low cost laminates.
Finish	No good universal Pb-free finish available. Conditions include tin whisker risk, corrosive environment risk, shelf life, solderability, etc.
Number of reflows required	Specify sufficient requirements to accommodate manufacturing, rework and repair solder reflows.
Number of thermal cycles	Require thermal cycle sufficient to meet manufacturing, rework, repair and service life.

Issue	Considerations
Copper dissolution resistance requirements	Require sufficient surface copper thickness to accommodate manufacturing, rework, and repair.
Manufacturability	Perform all of the above and still maintain manufacturability.
CCA	
Design solder stress levels	Pb-free solder stress design rules are not defined. Allowable stress is dependent on loading (thermal, vibration and shock), solder alloy, part type, part size, part placement and PCB design.
Placement of parts	See “Designed solder stress levels.”
Manufacturability	Manufacturing processes and rework method influences parts selection and placement.
Sustainment	Repair has considerations similar to rework.
Tin whisker mitigation	Amount of tin area, tin conductor spacing, conformal coating, etc. Whisker mitigations not linked to reliability numbers.

■ Low Risk/Mature    ■ Medium Risk/Moderate Maturity    ■ High Risk/No Maturity

**Table 3.2** Summary of key design considerations.

*Notes: CTE = coefficient of thermal expansion; MSL = moisture sensitivity level*

#### 3.1.2 Closure

Design processes used for heritage SnPb assemblies need to be modified to address Pb-free solder and finish selection in terms of fatigue characteristics, tin whisker risk, tin pest risk, rework, PCB reliability, copper dissolution, and SnPb compatibility. There are many knowledge gaps that need to be filled in order to consider using Pb-free solder over a broad range of A&D product service environments. Since there is a significant lack of Pb-free A&D product data in service, it is recommended that candidate path finder products be identified, characterized and introduced into low risk, low stress A&D applications. Assembly and repair solder alloys need to be defined in the design documentation.

### 3. Design

A significant difference between consumer and A&D products are that A&D products take a significantly longer period of time between the establishment of customer qualification requirements and the qualification testing. Typically, a three to five year period can elapse before the two are reconciled, and it is likely that in the interim, a new and better Pb-free solder alloy will have been developed, new failure modes encountered, and test practices optimized.

To aid risk assessment, a number of GEIA standards and handbooks have been released addressing performance, tin whiskers, test, technical considerations (including design), program and system engineering management, and repair/rework. While these documents do not yet address all issues, they are under constant review and assessment, and updated as more data and information become available. Table 3.3 summarizes these resources.

<div><input type="checkbox"/> GEIA-STD-0005-1, Performance Standard for Aerospace and High Performance Electronic Systems Containing Pb-free Solder [4] Used by aerospace electronic system “customers” to communicate requirements to aerospace electronic system “suppliers.”</div>
<div><input type="checkbox"/> GEIA-STD-0005-2 [5], Standard for Mitigating the Effects of Tin in Aerospace and High Performance Electronic Systems [5] Used by customers and suppliers to mitigate the detrimental effects of tin whiskers in high performance electronic systems.</div>
<div><input type="checkbox"/> GEIA-STD-0005-3 [6], Performance Testing for Aerospace and High Performance Electronic Interconnects Containing Pb-free Solder and Finishes [6] Used by customers and suppliers for direction and guidance for the performance testing of electronic assemblies that utilize Pb-free solder interconnections.</div>
<div><input type="checkbox"/> GEIA-HB-0005-1, Program Management/Systems Engineering Guidelines for Managing the Transition to Pb-free Electronics [7] Used by program managers to address all issues related to Pb-free electronics, e.g., logistics, warranty, design, production, contracts, procurement, etc.</div>
<div><input type="checkbox"/> GEIA-HB-0005-2, Technical Guidelines for Aerospace and High Performance Electronic Systems Containing Pb-free Solder [8] Used by customers and suppliers to select and use Pb-free solder alloys, other materials, and processes. It may include specific solutions, lessons learned, test results, data, etc.</div>
<div><input type="checkbox"/> GEIA-HB-0005-3, Rework/Repair Handbook to Address the Implications of Pb-free Electronics and Mixed Assemblies in Aerospace and High Performance Electronic Systems [9] Used by customers and suppliers for guidance on the repair/rework of electronic assemblies including mixed (Pb-free and SnPb) systems.</div>

Table 3.3 Summary of released GEIA Pb-free risk mitigation resources.

Particularly pertinent to the designer, the GEIA-HB-0005-2, *Technical Guidelines for Aerospace and High Performance Electronic Systems Containing Pb-free Solder* captures Pb-free design considerations and lessons learned applicable to A&D products (Table 3.4).

1	Scope
2	References
3	Terms and Definitions
4	Approach
5	General Pb-Free Solder Alloy Behavior
	<ul style="list-style-type: none"> <li>5.1 Elevated Temperature</li> <li>5.2 Low Temperatures</li> <li>5.3 Temperature Cycling</li> <li>5.4 Rapid Mechanical Loading (Vibration/Shock)</li> </ul>
6	System Level Service Environment
7	High Performance Electronics Testing
8	Solder Joint Reliability Considerations
	<ul style="list-style-type: none"> <li>8.1 Mixing of Solder Alloys and Finishes</li> <li>8.2 Pb-Free Terminations in SnPb Joints</li> <li>8.3 SnPb Terminations in Pb-free Joints</li> <li>8.4 Bismuth Effects</li> <li>8.5 JCAA/JGPP Testing of Mixed Alloy Combinations</li> <li>8.6 Pb-Free Solder and Mixed Metallurgy Modeling</li> </ul>
9	Piece-Parts
	<ul style="list-style-type: none"> <li>9.1 Materials</li> <li>9.2 Temperature Rating</li> <li>9.3 Special Considerations</li> <li>9.4 Plastic Encapsulated Microcircuit (PEM) Moisture Sensitivity Level (MSL)</li> <li>9.5 Terminal Finish</li> <li>9.6 Assembly Stresses</li> <li>9.7 Hot Solder Dipping</li> </ul>

### 3. Design

---

---

10	Printed Circuit Boards
10.1	Plated Through Holes
10.2	Copper Dissolution
10.3	PCB Laminate Materials
10.4	Surface Finish
10.5	Pb-Free PCB Qualification
10.6	PCB Artwork and Design Considerations for Pb-Free Solder Applications
11	Printed Circuit Board Assembly
11.1	PCB Process Indicator Coupons
11.2	Solder Inspection Criteria
11.3	Fluxes, Residues, Cleaning and SIR Issues
12	Module Assembly Considerations
12.1	Connectors and Sockets
12.2	Heatsinks/Modules
12.3	Conformal Coating
13	Manufacturing Resources
14	Aerospace Wiring/Cabling Considerations
14.1	Insulation Temperature Rating
14.2	Cable Connectors
14.3	Wire Terminals
14.4	Splices
14.5	Sleeving
15	Rework/Repair
15.1	Piece Part Rework
15.1.1	Area Array Rework
15.1.2	Surface Mount Capacitor/Resistor Rework
15.1.3	Through-Hole Piece Part Rework
15.2	Depot Level Repair
15.3	Mixed Solder Rework Temperature Profiles
15.5	Rework/Repair Cleaning Process
15.6	Inspection Requirements



16	Generic Life Testing
16.1	Thermal Cycling, Vibration and Shock Testing
16.2	Other Environments
16.2.4	Generic Humidity
17	Similarity Analysis
App A	Equipment Service Environmental Definition
A1.	Service Cyclical Temperature Environments
A2.	Steady Temperature Service Environments

Table 3.4 Design sections in GEIA-HB-0005-2 for Pb-free risk management.

These are industry documents where key published findings have been extracted and added to other significant, complementary information ascertained through A&D participation. The GEIA documents outline areas where data consensus exists, where there is conflicting data, and a lack of data.

Designing for Pb-free is a significant challenge and the information conveyed in this report is presented to help distinguish *current baseline practices*, identify *gaps/issues*, and provide *recommendations* for future road-mapping and planning.

3.2 REQUIREMENTS

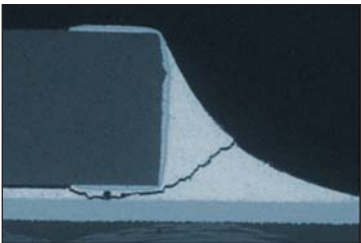
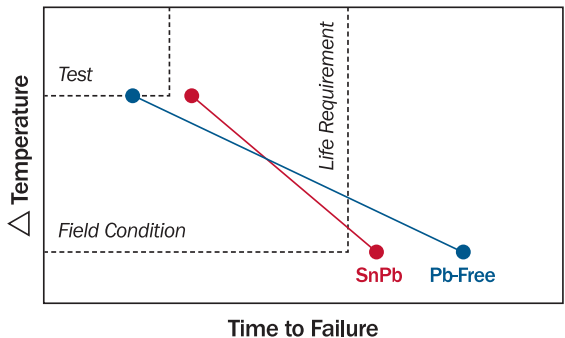
Customer requirements are the driver behind product/system design and manufacturing. Acquisition reform practices have resulted in more performance based requirements to suppliers with less, if any, focus on how the product is to be produced and sustained. Since Pb-free solder is not consistently “as good or better” than SnPb solder, A&D suppliers will face challenges in meeting customer requirements (Figure 3.3).



Fatigue under changing thermal conditions. At high strain levels (temperature extremes), tin-lead solder outperforms lead free solder.

### 3. Design

Durability of solder under a temperature cycle.



Studies have shown that lead free solder alloys fail at loads up to 50% lower than tin-lead solder when shocked, dropped or bent. Photo courtesy of CALCE, UMD.



For explosive and drop shock, lead free solder is more likely to fail than tin-lead solder.



**Figure 3.3** Environmental conditions and their impact on A&D performance.

In product systems, Pb-free risks can manifest themselves as an increase in short circuits, open circuits and intermittent circuit failures (Section 7.0, Reliability). Pb-free is introduced into the product stream through parts which have integrated internal features, part finishes, PCB finishes, and assembly solders. The impact of Pb-free is treated with characteristically similar skepticism, which is intrinsic to the introduction of any new technology where a lack of historical data can hinder an empirical decision making process. Pb-free impacts many facets of the requirements hierarchy and electronic hardware design process (Figure 3.4).

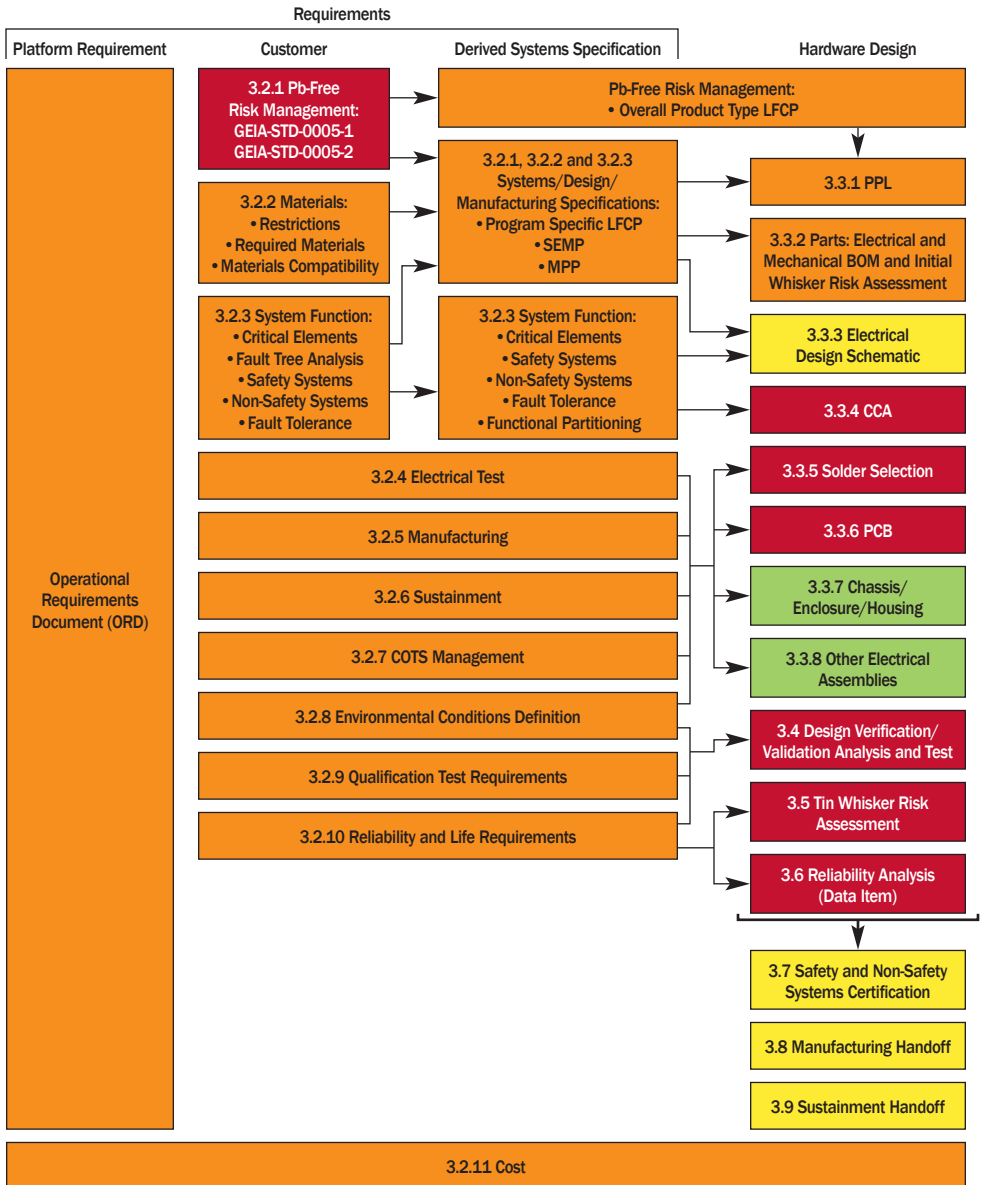


Figure 3.4 Requirements and design elements impacted by Pb-free. Note the risk color coding is based on having both Pb-free finished parts and Pb-free soldered assemblies. The various relevant section numbers are provided for the requirements and design elements herein.

### 3. Design

---

*Notes: ORD = operational requirements document; LFCP = lead free control plan;  
SEMP = systems engineering management plan; MPP = materials and processes plan;  
PPL = preferred parts list; BOM = bill of materials*

The customer, systems and hardware requirements impacted by Pb-free finishes and assembly solder alloy are discussed next.

#### 3.2.1 Pb-Free Risk Management Requirements

##### *Current Baseline Practice*

At the present time, there is a broad variation in customer requirements and design practices regarding Pb-free risk. Nevertheless, Pb-free control plans are being developed by many customers and suppliers to manage Pb-free risk.

The current Baseline Practice of Pb-free risk management transcends a wide spectrum of responses from “unaware” to “ambivalent” to “extremely concerned” with many intermediate positions in the continuum. The Pb-free risks are manifested at a systems level in terms of interconnect reliability of the Pb-free solder and the PCB, and tin whisker risk associated with the part finishes and Pb-free solder. In addition, most Pb-free solders currently in use have higher melting points than tin/lead solder, and require higher processing temperatures which can damage components and PCBs.

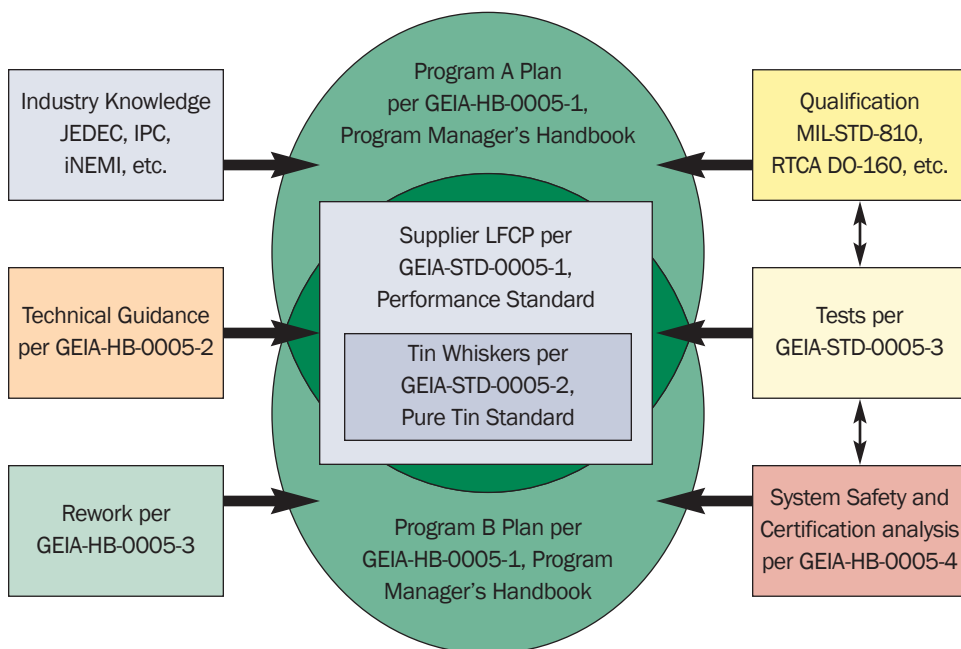
One approach that has emerged to manage the Pb-free risk is to utilize the GEIA Pb-free risk management standards and handbooks (GEIA-STD-0005-1, GEIA-STD-0005-2, GEIA-STD-0005-3, GEIA-HB-0005-1, GEIA-HB-0005-2, and GEIA-HB-0005-3).

One means of satisfying GEIA-STD-000-1 is to create a Pb-free control plan (LFCP) that defines the practices used across design, manufacturing, procurement, and sustainment to manage the Pb-free risks. A Pb-free control plan can be written at many levels. At the highest level, it defines the overall processes of Pb-free risk management. Individual programs can also have plans that tailor the overall strategy to accommodate unique program requirements.

The LFCP is a document that defines:

- Allowable Pb-free finishes and solders.
- Sources of reliability data.
- Product configuration and identification.
- Compatibility with heritage SnPb solder.
- Tin whisker mitigations.

The LFCP can utilize many sources of data including the Pb-free documents shown in Figure 3.5.



**Figure 3.5** How the GEIA Documents work together.

#### Issues/Gaps/Misconceptions

There are several issues associated with these standards:

1. Gap: Existing programs often lack funding for Pb-free risk mitigation, and without informed customer direction, these programs will continue to be measured on unrealistic cost and schedule objectives. The increased costs associated with non-tangible Pb-free risk mitigation activities require substantial efforts to justify, and in some cases, these justification efforts may actually exceed the implementation of the actual mitigation.
2. Misconception: In contrast to a prescriptive specification, GEIA-STD-0005-1 does not tell a designer “what to do,” rather it requires definition of the processes by which reliability, configuration, and sustainment are maintained while Pb-free is accommodated in their product.

### 3. Design

---

3. Gap: Since the GEIA standards are based on incomplete technical knowledge, there continues to be significant changes as new information is obtained. One of the challenges is that there still remains a substantial void of quantifiable reliability data for vibration, shock and combined thermal cycling/vibration/shock as it pertains to the use of Pb-free solder in most A&D applications.
4. Misconception: One misconception is that the use of any – or all – of these documents implies that A&D *does not* imply that A&D condones the use of Pb-free technology. Rather these documents are used to mitigate risks associated with Pb-free for situations in which the supplier/customer has no other alternative than to use Pb-free components and assemblies (e.g., COTS items).
5. Issue: The means by which a company can certify to GEIA-STD-0005-1 is not established. At the present time, a combination of self certification and customer certification is used.
6. Issue: The procedure for change management of the Pb-free control plan has not been determined. It will not be possible to obtain optimal reliability and maintain rapid change responses for high risk Pb-free findings if every A&D customer demands LFCP approvals before a change can be implemented.
7. Gap: GEIA-STD-0005-2 is a system of methods to manage the tin whisker risk but does not eliminate the risk. SnPb solder dipping, conductor spacing control, and conformal coating have been the most broadly utilized means to mitigate whiskers; however, the present state of the art does not allow quantification of these mitigations on overall system reliability.
8. Misconception: There is a general relationship between the GEIA-STD-0005-2 tin whisker risk mitigation level selection and the types of parts/assemblies upon which the program costs are based. As shown in Table 3.5 and Table 3.6, at level 2C or above, the parts are typically listed on custom control drawings and are not generally COTS. The majority of A&D products fall into a class 2A or 2B regime.
9. Misconception: Another poorly understood aspect of tin whisker risk is that the tin whisker growth clock starts ticking once the assembly process has been completed. Thus, a spare assembly which sits on the shelf for an extended period of time can grow significant whiskers. Consequently, periodic inspection/remediation may be necessary to ensure availability.
10. Gap: Customer requirements and systems engineering management plans do not often include sufficient detail for Pb-free risk management, such as definition of GEIA-STD-005-2 level requirements, COTS requirements, and sustainment requirements.

GEIA-STD-0005-2 Level	Risk Control Mechanisms
3	Control tin risk exclusively by tin avoidance
2C	Control tin risk predominantly by tin avoidance, and in exceptional cases by design rules
2B	Control tin risk predominantly by design rules, and in exceptional cases by tin avoidance
2A	Control tin risk exclusively by design rules
1	Tin risk uncontrolled

Table 3.5 GEIA tin whisker mitigation levels.

GEIA-STD-0005-2 Level	Part Type		Assembly Type	
	Special Parts	COTS Parts	“MIL-COTS” Assembly	True COTS Assembly
3	yes	no	no	no
2C	yes	by exception only	no	no
2B	yes	yes	yes	no
2A	yes	yes	yes	yes
1	yes	yes	yes	yes

■ Low Risk ■ Moderate Risk ■ A&D High Risk

Table 3.6 GEIA-STD-0005-2 Level Selection and Part/Assembly Type

### Conclusions

The Pb-free control plan is an integral part of ensuring the reliability of complex systems that are faced with the depleting supplies of Pb in electronic materials. The key feature of the LFCP is that it coordinates the Pb-free roles and responsibilities of the design, configuration, manufacturing, procurement and sustainment functions.

### 3. Design

---

#### *Recommendations*

1. The use of a LFCP to manage Pb-free risk should be considered a best practice.
2. Implement a formal review cycle for each of the GEIA documents to accommodate the continuous increase in release of new alloys and associated data.
3. Develop a uniform process for GEIA-STD-0005-1 certification.
4. Develop a procedure for Pb-free control plan change management.
5. The customer requirements and the systems engineering management plan (SEMP) need to capture specific Pb-free risk mitigation requirements for the program.
  - Tin whisker risk: Regardless as to whether the assembly uses SnPb or Pb-free solder, the Pb-free risk from components should be acknowledged and the appropriate GEIA-STD-0005-2 tin whisker mitigation level should be defined.
  - Sustainment requirements: The sustainment and repair requirements such as compatible repair solder alloys should be defined where appropriate.
6. Through test and analysis, develop methods to quantify tin whisker risk mitigations on overall system reliability.
7. Include an approach to account for tin whisker growth on assemblies during the time between manufacturing and use.
8. Promote active Pb-free risk management by continuing industry activities in research, technology monitoring, and the assessment of new data as it becomes available.

#### **3.2.2 Materials Requirement**

##### *Current Baseline Practice*

Materials include electronic assembly items such as solder alloys, PCB finishes, electronic components, internal and external materials, surface finishes and metal part finishes. Materials requirements often include (1) restricted and prohibited material lists (e.g., hazardous material or HAZMAT), (2) fluid compatibility and (3) required materials. Allowable solder materials are often contained within manufacturing requirements such as: J-STD-001 and J-STD-006, which are the main manufacturing standards for acquisition of electronic assemblies. Restricted materials are identified per local, state, and/or national regulations. However, the electronics industry is directly affected by world-wide legislation, primarily the European Union's RoHS regulation [10]. Other regulations (Table 3.7) are also generating an impact on material usage but are outside the scope of this current baseline practice study.



Standard/Regulation	Type	Impact
U.S. HR Bill 2420	Global	Contains elements similar to RoHS. It currently has no exemption language for military and aerospace products. It prevents states from enacting individual restricted materials legislation for electrical and power distribution equipment. The advocacy group of the AIA-PERM consortium is working on this.
U.S. Executive Order (EO) 13423	Affects acquisitions by "federal agencies"	Contains requirements for compliance to EU RoHS. As "an executive order" It has the force of U.S. law, but since RoHS doesn't apply to defense, the EO does not affect procurement of military electronics by DoD.
RoHS	Global	Prohibits use of elemental lead in certain product categories, most of which impact A&D in terms of COTS items that are acquired. While A&D are excluded, impact is still felt from COTS usage.
"Japan" RoHS	Global	Does not necessarily ban use of elemental lead, but does impose "disposal" fee on manufacturers.
"Korea" RoHS	Global	Somewhat consistent with the EU's RoHS, but Korea RoHS does not require labeling of product as compliant. Korea RoHS also has a recycling provision that is more "prescriptive" from the EU's WEEE directive.
"China" RoHS	Global	Uses a catalog that identifies all Electronic Information Product (EIP) under the China RoHS guidelines. The implementation responsibility falls upon the manufacturer and the importer of the EIP. Many product types that are not within the scope of EU RoHS are within the scope of China RoHS, including automotive electronics, radar equipment, medical devices, semiconductor and other manufacturing equipment, components, some raw materials, and some packaging materials. Implements test requirements by approved laboratories on products to verify compliance to material limits via a catalog approach.

3. Design

Standard/Regulation	Type	Impact
California	State	SB 20 contains both RoHS and WEEE-like provisions. The only substances restricted are “certain heavy metals,” specifically lead, mercury, cadmium and hexavalent chromium. In contrast to the EU, California does not restrict PBB and PBDE.

■ No Impact to A&D   ■ Minimal Impact to A&D   ■ Major Impact to A&D

Table 3.7 Summary of regulations affecting elemental lead usage.

The materials allowed in the final systems requirements is a synthesis of the standard materials used within a manufacturer’s processes, and the customer’s allowable materials. Materials and process plans (MPP) or system engineering management plans (SEMP) can be used to coordinate materials use on a program.

Issues/Gaps/Misconceptions

1. Issue: Regulatory agencies are banning/limiting materials without due diligence with respect to industry performance and product impact.
2. Issue: Use of Pb-free finishes can exacerbate the tin whisker phenomena.
3. Misconception: There are environmentally safe drop-in replacements for SnPb solder; this is not the case.
4. Issue: Recently, the number of materials on restricted/prohibited lists has grown dramatically due to various legislative activities and executive orders. There are increasing numbers of customers and programs that are specifying materials being used in electronic systems based on “boiler plate” language derived from other types of equipment. For example, it is unreasonable to expect that an electronic assembly can be made without a nickel plated layer, which is an essential barrier material for dissolution and diffusion, and for which there is no replacement
5. Issue: Managing an extensive restricted and prohibited materials list for electronic products is a very challenging task because electronic assemblies are comprised of many thousands of parts from hundreds of suppliers. Certifying compliance to restricted and prohibited materials lists can be quite costly if all the data from the piece parts is not collected up front in the part selection process. Evaluating the extensive lists of restricted materials can result in a costly review process that should be accounted for during project planning and contracting.

6. Issue: Solder materials are often specified indirectly when electronic assembly soldering is required in accordance with J-STD-001. Unfortunately, J-STD-001 allows for multiple Pb-free alloys under certain conditions, which may not give sufficient guidance for sustainability considerations.

#### *Conclusions*

Presently, there is no drop-in environmentally conforming Pb-free solder that meets the SnPb current baseline practice for performance and reliability. Some Pb-free alloys show comparability with SnPb under certain limited service conditions, but no one material has yet to meet SnPb current baseline practice performance.

#### *Recommendations*

1. It is recommended that the review of material requirements with hardware design, manufacturing, and environmental health and safety (EHS) be performed as early as possible in the systems planning, contracting, and design cycle.
2. Systems engineering management plan requirements should mandate that solder alloy materials be part of the design documentation, part of COTS requirements, and the sustainment package.
3. It may be advantageous to accumulate the materials data for electronic parts in a database.
4. *Restricted and prohibited materials:* It is important to work with customers early in the proposal process to review the true health concerns as it pertains to the use of these materials in electronics. Restrictions on the use of lead (Pb) may be encountered in this section.
5. *Required materials:* In the future, it is recommended that customers will specify specific solder alloys for assemblies in order to reduce proliferation of solder alloys needed in repair.
6. *Materials compatibility list:* It is recommended that customers require compatibility with other materials.
7. Encourage research to develop a Pb-free alloy (per RoHS regulated acceptable materials) that meets or exceeds eutectic SnPb performance and reliability requirements (thermal cycle, vibration, mechanical shock).
8. Generate design guidelines (at CCA, box, unit or other COTS-item level) to close the performance gaps.

### 3. Design

- 9. For sustainability reasons, encourage platform and customer guidance on compatibility requirements for solder repair alloys. Note that if the repair alloy is different from the build alloy, it may be necessary to perform additional analysis and/or qualification testing to substantiate the mixture of as-built and repair alloys.

#### 3.2.3 System Criticality Requirements

##### Critical Elements of Safety Systems and Non-Safety Systems

###### Current Baseline Practice

At the present time, electronics systems are broken down into two major classes (1) non-safety systems and (2) safety systems. The non-safety critical systems will have reliability requirements.

While the safety systems require systems safety analysis utilizing a combination of fault trees, FMECA, etc., linkage of circuit functions to severity for military/DoD programs is made through the standard practice for systems safety (MIL-STD-882) and FMEA (MIL-STD-1629A).

For commercial programs, failure conditions are identified per the system development process (SAE ARP4754) and the system safety assessment (ARP4761; FAA AC25.1309) and others.

A typical proactive systems safety program is outlined in Figure 3.6. This is the place where failure distributions driven by Pb-free changes will be observed at the design level.

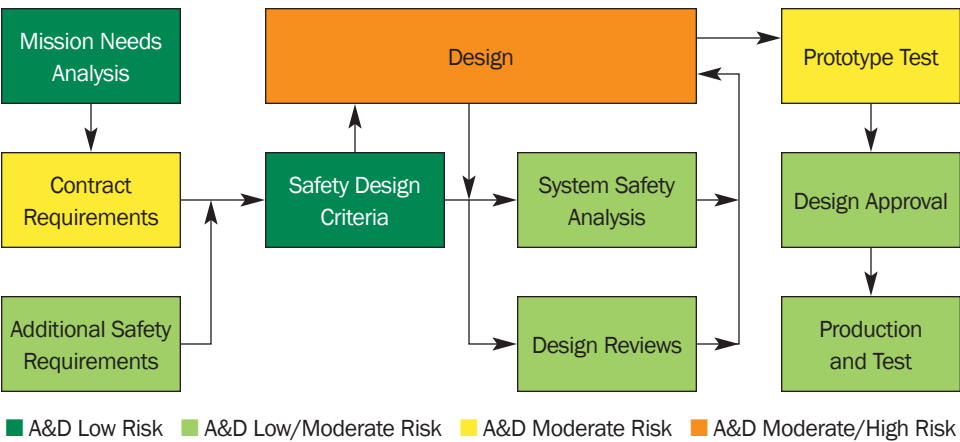


Figure 3.6 Typical proactive systems safety program [Source: FAA Systems Safety Handbook 2000].

#### *Issues/Gaps/Misconceptions*

Issue: The additional safety requirements, design reviews and the system safety analysis process may need updates for Pb-free considerations.

#### *Conclusions*

A set of comprehensive specifications are currently used to govern system safety analysis.

#### *Recommendations*

1. It is a technical imperative that safety systems add GEIA-STD-0005-1 to the appropriate standards that are used to assure A&D systems safety.
2. Recommend review and/or update of MIL-STD-882 and other related systems safety standards for consistency.

### **Pb-Free Considerations During Fault Tolerance Assessment**

#### *Current Baseline Practice*

At the present time, the following Pb-free impacted items are routinely addressed in the fault tolerance assessment:

- FTA (Fault Tree Analysis)
- FMEA (Failure Mode and Effects Analysis) for non-systems safety products
- FMECA (Failure Mode, Effects, and Criticality Analysis) for systems safety products
- Short circuit and open circuit condition qualitative/quantitative risk assessment
- Intermittence during start-up and steady state operation risk assessment

The FMECA/FTA typically looks at a single failure at a time and its effects on the system. There could be multiple tin whisker failures that occur clustered together in time if (some of) the factors that promote whisker growth are common. (Note: This is not unique to tin whiskers; it's true in other cases, such as instances where fault conditions result from multiple parts from the same defective lot present in a unit.) Whisker risk factors such as a production run of possibly defective tin plating on the same lot of parts, exposed to the same environment, side by side on the same board, could contribute to multiple failures clustered together. But there are still likely to be many other factors that randomly affect the time to failure, such as growth rates (spurts), geometric angle, distance to the nearest lead/conductor, and conformal coat thickness and hardness. So the risk may be more akin to multiple faults, or multiple intermittent faults, as opposed to a common fault affecting two or more circuits simultaneously.

### 3. Design

---

---

As time goes on, tin whisker risk is expected to increase as the tin regions have greater opportunities to grow. At some point, tin whisker shorts may increase in frequency and approach more of a “common cause,” or have nearly simultaneous single failures that look like multiple failures. However, the field failure trends should provide data on the rate of whisker failure occurrence, and allow adjustments to be made in maintenance schedules to ensure continued safe operation.

#### *Issues/Gaps/Misconceptions*

1. Issue: Currently, Pb-free failure modes are not part of the table of failure modes which may result in the following:
  - Challenging fault tolerance assumptions.
  - Assumption of one failure at a time may be challenged.
2. Gap: Pb-free aggravates fault rates to varying extents for the following failure modes:
  - Short circuit modes:
    - New: pad cratering leading to electrical leakage, tin whisker bridging, metal vapor arcing high energy short.
    - Made worse: Higher temperature processing may increase solder defects or incidence of CAF, low surface insulation resistance, cracks in moisture sensitive components, component warpage (e.g., area array head-in-pillow solder joints), or multilayer ceramic capacitor cracks.
  - Open circuit modes:
    - New: Pad cratering leading to fractured PCB conductor.
    - Made worse: PCB delamination, solder joint failure, intermetallic failure, surface trace failure, PTH/via failure, inner trace failure, solder electromigration, open following high energy short.
  - Intermittent open/short circuit modes:
    - The intermittent as a class of failure has been a significant challenge to historic FME. Introducing large numbers of intermittent failures may result in a re-examination of the FME analysis activity. Most mechanical fractures exhibit intermittent open circuit conditions prior to manifesting itself as a full open circuit. In addition, tin whisker failures usually manifest themselves as intermittent short circuit conditions to neighboring connections.
    - Intermittent failure conditions are often masked as no-fault-found during troubleshooting during returned hardware assessment.

With the anticipated increase of Pb-free related failures, at least for a period of time, the risk factors may increase the system fault burden to varying degrees, depending upon the functional circuit element design, the environmental conditions, the whisker mitigations and the maturity of the Pb-free assembly process.

#### *Conclusions*

The fault tree and FMEA/FMECA analysis is well established for many programs and the fundamental method of analysis is unchanged for Pb-free. There are expected to be greater incidence of short circuit, open circuit, and intermittent connections especially during the early introduction of Pb-free interconnect technologies.

#### *Recommendations*

The following items are recommended:

1. Systems engineering must work with reliability to identify and quantify the contributions of Pb-free technology to the short circuit, open circuit, and intermittent Pb-free failure modes.
2. The tin whisker risk shorting failure mode ranges from intermittent, to fixed shorting, to catastrophic arcing and needs to be added to the table of failure mode types in order to facilitate subsequent FME analysis.
3. It is imperative that an adequate level of field failure monitoring and failure analysis is instituted so that an increase in failure rate due to tin whiskers would be captured.
4. Product design engineering should consider changes to the failure rates associated with higher processing temperatures necessitated by Pb-free solder that will reduce process windows during soldering, and increases in assembly complications due to tin whisker mitigations.
5. Environmental stress screening (ESS) test plans should consider applicable Pb-free failure modes for screening of infant mortal defects.

#### **Pb-Free Considerations During Functional Block Definition**

##### *Current Baseline Practice*

Assessing and assigning tin whisker risk level may be done at the system, the line removable module LRU, and/or the CCA. The more costly and extensive tin whisker risk mitigations are often integrated into the design as a function of the circuit element group criticality.

### 3. Design

---

---

#### *Issues/Gaps/Misconceptions*

Gap: The link between tin finish and Pb-free solder use, on a particular function circuit element, occurs at various stages of the design but is often not captured sufficiently in a searchable database.

#### *Conclusions*

The system functional block assignment process is an established, robust process that can be updated to accommodate tin whisker risk management.

#### *Recommendations*

It is important to track circuit element groups to facilitate updates to the tin whisker risk mitigation approaches and changes to Pb-free risk assessment, if additional Pb-free failure modes are encountered.

#### **3.2.4 Electrical Testing Requirements**

The focus is on finding opportunities for improvement in fault (including intermittent) coverage.

#### *Current Baseline Practice*

Testing is performed in accordance with processes and/or procedures cited in specific contract or statements-of-work. Many of the current test instruments utilize digital processing of signals. While digital measurements may be highly accurate when the source measured is stable and/or repetitive, in cases where the source is intermittent, noisy or unstable, it is an entirely different matter. To smooth these noisy and randomly changing signals, digital averaging is used and as a result, a portion of the unexpected intermittent defect may not be observed. This will depend on the frequency and duty cycle of these glitches [11]. The inability of improperly designed System/LRU/CCA self test and/or test equipment to catch intermittent conditions, is likely to contribute to increasing the rate of no fault found (NFF) conditions, where users report failures that are not replicated on the ground during testing.

#### *Issues/Gaps/Misconceptions*

Issue: There is a concern that electrical intermittent failures may not receive the level of attention that is warranted. One common failure mode, manifested by whiskers, is intermittence. Such phenomena can be a major concern for high reliability-required systems, e.g. safety and mission critical requirements. New failure mechanisms exist with Pb-free alloys, and they can manifest themselves as latent field failures not discovered by testing.



### *Conclusions*

The improved detection of intermittent electrical phenomena, from tin whiskers and other Pb-free failure mechanisms, can help avoid potentially catastrophic failures.

### *Recommendations*

1. Develop built in test and external test methodologies to improve the capture of intermittent electrical operations.
2. Generate a methodology to assess tin whiskers as a source of intermittent electrical phenomenon.

## **3.2.5 Manufacturing Requirements**

Within performance-based acquisition, customer-imposed manufacturing requirements are few in number. However, in high reliability systems, such requirements are a necessity to address concerns from materials (e.g., presence of pure tin), soldering, and others.

### *Current Baseline Practice*

Material requirements can include prohibition of pure tin surface finishes. Operational requirements may include use of J-STD-001 for soldering as well as customer-specific (via contract or statement-of-work) requirements.

### *Issues/Gaps/Misconceptions*

1. Issue: It is an issue for A&D programs that J-STD-001 allows for multiple Pb-free alloys under certain conditions, which may not give sufficient guidance for sustainability considerations.
2. Issue: The mixed alloy situation that results from using Pb-free ball grid array (BGA) components with a SnPb soldering process, will require attention as material selection/processes appear to be supplier specific (Manufacturing Section 4.6).

### *Conclusions*

J-STD-001, the umbrella standard for soldered assemblies, allows solder alloys other than Sn60A, Pb36B, and Sn63A to be used, provided that the required electrical and mechanical attributes and all other conditions of J-STD-001 standard are met, and objective evidence of such is available for review. Thus in principle, multiple Pb-free alloys can be used, but they may adversely impact repair during sustainability.

### 3. Design

#### Recommendations

1. An update to J-STD-001 is needed, to improve the definition of “objective evidence” where Pb-free solder is used in place of SnPb. Pb-free solder is an emerging technology for high reliability applications. Changes to J-STD-001 need to be considered immature until sufficient data is available to prove the integrity of the new requirements.
2. Additional data must be acquired by performing Pb-free rework/repair reliability studies, some of which are presently underway.

#### 3.2.6 Sustainment Requirements

##### Current Baseline Practice

Sustainment includes supply chain, integrated logistics support, and repair as is illustrated in Figure 3.7.

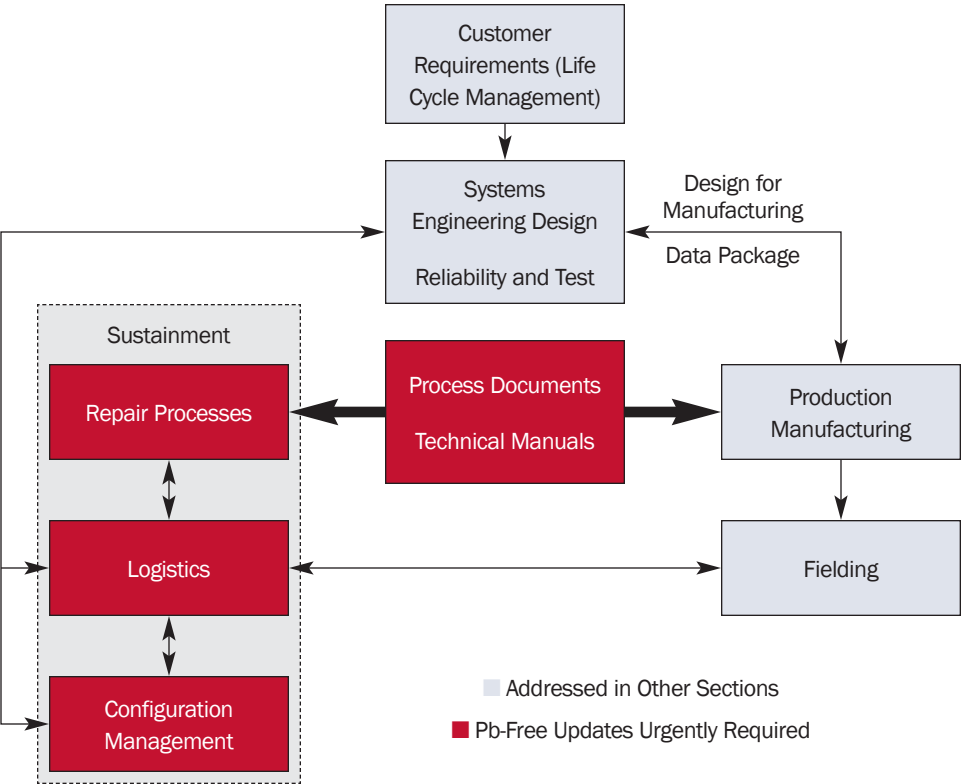


Figure 3.7 Sustainment Impact. Introduction of Pb-free materials and processes will require significant changes in sustainment practices.

Customer requirements that define the logistics program have evolved over time to accommodate primarily SnPb assemblies. The general systems requirements define appropriate elements, but some specific concerns for Pb-free assemblies exist. Some standards and guidelines have been released (J-STD-609) to address component marking/identification but these are not mandatory within the commercial industry. For repair, GEIA-HB-0005-3 has been released for guidance on repair/rework of Pb-free for A&D equipment.

#### *Issues/Gaps/Misconceptions*

1. Issue: Supply chain, integrated logistics support, and repair processes are executed per program-specific (which may include military or federal standards) requirements. To date, none of these practices has undergone standard modifications or adaptations for Pb-free.
2. Issue: Design interface. The incorporation of Pb-free introduces the potential use of a wide variety of materials and processes that have significant effects on logistics requirements, particularly repair practices and spare part materials procurement. Construction and layout of assemblies impacts maintainability and repairability. The interface between logistics disciplines and the design authority should address particular Pb-free issues.
3. Gap: Differentiation in part marking/identification for Pb-free is required.
4. Gap: Provisioning plans may need to include increased spare parts due to Pb-free performance shortfalls.
5. Issue: Customer repair facilities may require repair with only one Pb-free alloy.

#### *Conclusions*

The supply chain Pb-free transition will have profound impacts on all elements of sustainment. Present practices include the essential elements for assuring sustainment, but the materials properties and compatibility issues introduced by Pb-free assemblies will require major changes in the detailed implementation practices. Supply chain, logistics support, and maintenance organizations need guidance/direction in configuration management, spare part provisioning, and repair.

#### *Recommendations*

1. Implement Pb-free Control Plans in accordance with GEIA-STD-0005-1 broadly across the system supply chain.
2. Implement repair guidance such as GEIA-HB-0005-3 in the repair depots.
3. Formulate a supply chain strategy with focus on control of Pb-free components.

### 3. Design

---

4. System integrators need to require the use of a part marking standard for Pb-free if the specific solder material is part of the technical data package.
5. Consider aggressive preventative maintenance schedules with suitable spare parts to swap out units for examination, rework and repair.
6. Model and quantify repair costs and requirements using a model such as the one being developed by Dr. Peter Sandborn of University of Maryland CALCE EPS. The model is a Pb-free Electronics Use and Repair Dynamic Simulation [12]. Include Pb-free sustainability considerations in the customer requirements and the systems engineering management plan.

#### 3.2.7 COTS Assembly Management Requirements

##### *Current Baseline Practice*

In addition to circuit card assemblies manufactured by A&D OEMs or contract manufacturers, A&D programs incorporate purchased COTS assemblies into their products. Those assemblies may be categorized in a number of ways, but for purposes of this report, the two main categories are (1) those not within A&D control (NWADC), e.g., purchased disk drives, and (2) those within A&D control (WADC), e.g., Versa Module Eurocard (VME) circuit card assemblies. It is important for A&D users to assure the reliability of both categories in their applications. There is presently no current baseline practice for dealing with the impact of Pb-free electronics for these products.

##### *Issues/Gaps/Misconceptions*

1. Gap: Very little information regarding solder assembly materials or processes is available to the users of NWADC assemblies in the first category (*Current Baseline Practice*); furthermore, changes are made with little or no notification or visibility, and it is almost certain that the transition to Pb-free solder has been made in most of these assemblies.
2. Issue: The most obvious examples of the WADC second type of assembly (*Current Baseline Practice*) are the VME cards used mostly in military aerospace programs. VME BUS card manufacturers are strongly influenced by military requirements, but typically do not manufacture their products to the requirements of any specific program. The manufacturers of these assemblies work through their VITA organization (VMEbus International Trade Association). To date, there has been little involvement of these manufacturers in the Pb-free activities sponsored by various A&D organizations. This is identified as a serious gap.

#### Conclusions

A&D users have the responsibility to assure reliability of assemblies acquired from sources not within A&D control. They must do this with little information or assistance from the manufacturers. A&D users are in a position to influence the manufactures of the second category of assemblies listed under 3.2.7 (Current Baseline Practice).

#### Recommendations

1. The only way the users of NWDAC assemblies from the first category (*Current Baseline Practice*) can assure their reliability is to re-evaluate them periodically throughout the life cycle, and all users should do so. This re-evaluation may include:
  - Periodic inspection of incoming assemblies to identify the assembly materials and processes used.
  - Periodic re-qualification of the product with recently-received assemblies.
  - Periodic re-qualification of recently-received assemblies.
  - Periodic examination of in-service products for tin whisker formation.
  - Accessing all available information about the supplier and the product.
2. A&D program requirements for WADC assemblies in the second category (*Current Baseline Practice*) should be updated to include requirements to manage the use of Pb-free electronics. It is also recommended that all manufacturers of these assemblies be required to have Pb-free Control Plans, verified as compliant to GEIA-STD-0005-1.
3. Manufacturers of VME cards and other assemblies within A&D control should participate more actively in A&D Pb-free activities and whisker mitigation evaluations.

#### 3.2.8 Environmental Condition Specification

The environmental condition definition includes those service conditions that directly affect system/product performance during its intended use, including storage. The designer needs to evaluate the impact when assessing the performance of Pb-free at all levels (component, PCB, CCA) of product development. Also under consideration, should be the effects of tin whiskers as potential causes of failure. The degree of impact (e.g., safety, mission critical, etc.) needs to be considered, and mitigation plans must be appropriately generated. In cases where the customer has provided complete definition of the line replaceable unit (LRU) field conditions, these LRU level conditions must be translated to the CCA level using a combination of modeling, analysis and test to facilitate detailed solder stress analysis.

### 3. Design

---

---

#### *Current Baseline Practice*

Examples of typical environmental conditions are (Figure 3.3):

1. Temperature Requirements
  - Storage temperature excursions ranging from -55 °C to +125 °C
  - Normal mission temperature range
  - Cold day mission temperature
  - Hot day mission temperature
2. Vibration (airborne example)
  - Take-off
  - Cruise
  - Afterburner
3. Shock (airborne example)
  - Landing
  - Crash
  - Explosive
  - Gunfire
4. Humidity
5. Bench Handling and Shipping Drop Requirements

These design conditions are sometimes based on such standards/handbooks as MIL-STD-810, MIL-STD-1389, MIL-S-901, and others or derived from service data.

#### *Issues/Gaps/Misconceptions*

1. Issue: To date, equipment produced with any of the currently available Pb-free alloys has not demonstrated the ability to conform to all performance requirements.
2. Issue: Furthermore, COTS becomes a concern since the designer cannot control the components or materials used in the item.
3. Gap: Since most A&D products experience multiple service conditions, a combined environment test would be more practical and accurate in assessing compliance to performance requirements. However, the concept of combined environments is still a point of contention in the industry.

4. Gap: In cases where the environmental conditions are not defined, assumptions are often applied that can either result in significant added cost due to over design, or incorrect computation of solder joint life in actual service. For instance, a storage temperature of 125 °C is often specified, but duration is not given. While this may have been acceptable for SnPb soldered electronic assemblies, for Pb-free, intermetallic growth between the solder and the pad is more extensive and there may be increased incidence of intermetallic fracture under extensive high temperature aging. Alternatively, it is also true that Pb-free alloy material properties can change dramatically with extended aging that reduces subsequent thermal cycling reliability.

#### *Conclusions*

While some alloys have performed comparably to eutectic SnPb solder under limited stress levels, no one Pb-free material (characterized to date) has produced satisfactory results for all harsh environments. Additional analysis and testing is needed to determine requirements for testing and qualification of Pb-free alloys. During the introduction of Pb-free solder, an accurate accounting of the environmental conditions will improve the likelihood of Pb-free solder success.

#### *Recommendations*

1. As compared to SnPb, product built with Pb-free solder may have reduced margins, therefore the user and customer would benefit by obtaining concurrence on the final use environments rather than relying on traditional testing. This is a technical imperative.
2. A methodology or protocol should be established in which the customer/stakeholder and supplier collaboratively work to carefully select appropriate and accurate operating, transportation, and storage requirements.
3. Consider controlled storage of released equipment and/or development of an aggressive preventative maintenance schedule with suitable spare parts to swap out units for examination/rework/repair. A shorter warranty life cycle will be imperative.
4. Given that Pb-free solder is likely to be more sensitive to high stress conditions, it is important that accurate environmental conditions are provided early in the design process. The completeness of the environmental temperature, vibration, and shock condition specification varies considerably by customer and program.
5. In addition to the thermal and the mechanical dynamic environments, any humidity, corrosive gas, or salt fog test requirements should be specified.

3. Design

- 6. Utilize the guidance in GEIA-HB-0005-2 for the description of the service environments and the decomposition of these conditions to the circuit card level so that accurate solder stress modeling can be performed.

3.2.9 Qualification Test Requirements

Current Baseline Practice

Quite frequently, the successful completion of a formal qualification test is required as part of the contract performance. A summary of the qualification test types, goals and requirements is shown in Figure 3.8. In the present section, the product LRU (line replaceable unit) qualification is the focus of the discussion.

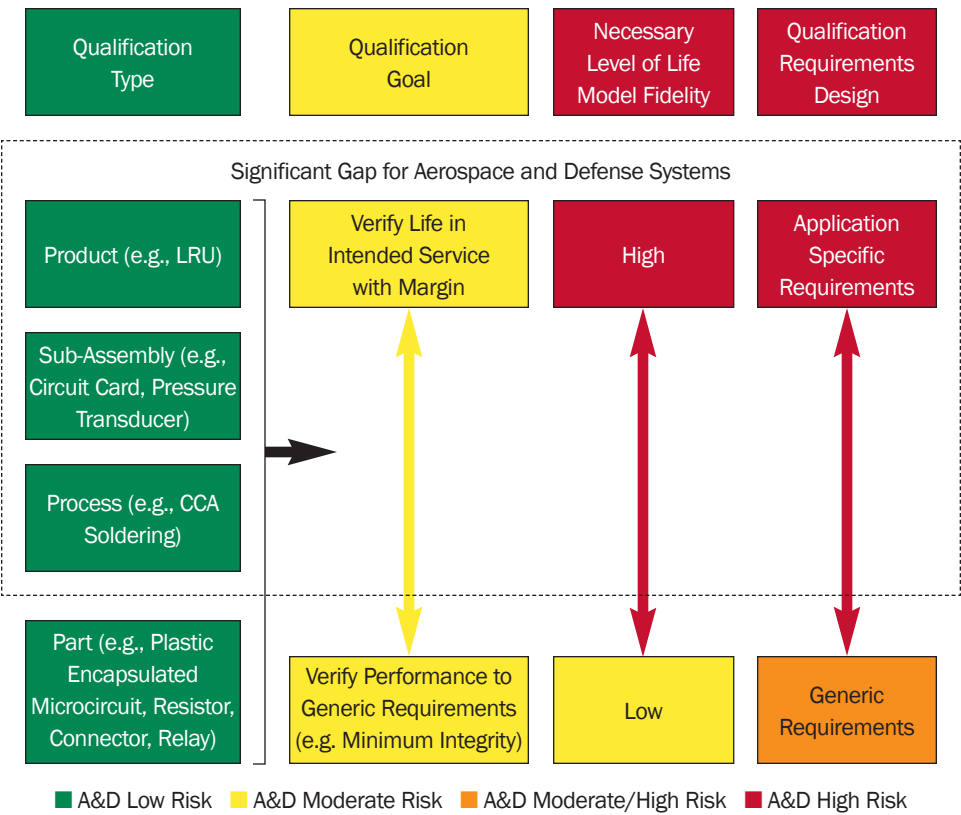
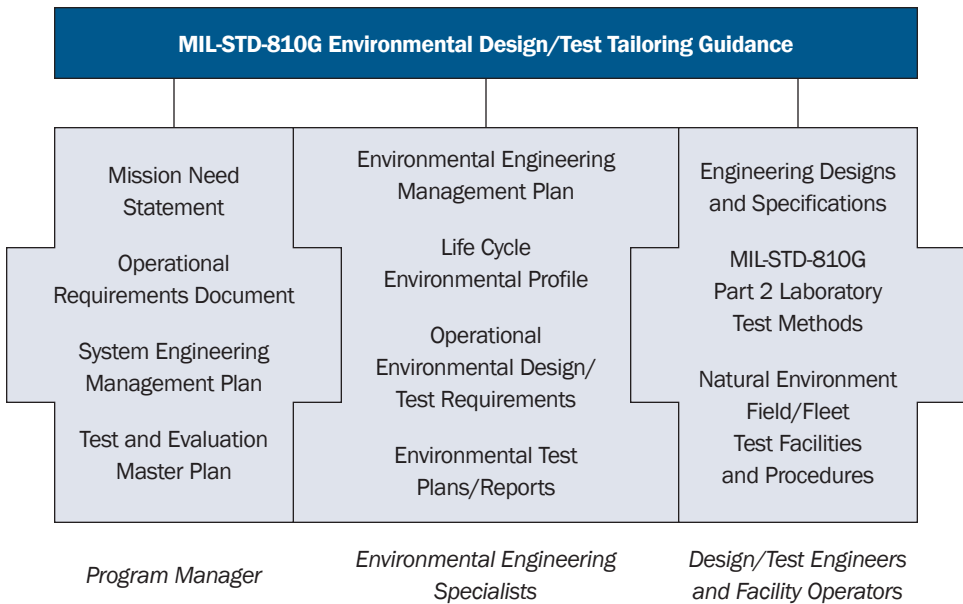


Figure 3.8 Typical qualification tests, requirements design and qualification goal.



A significant difference between consumer and A&D products is that three to five years can elapse between the time the qualification requirements are developed by the customer, and the time when the qualification test is performed. In that time, it is possible that a new and much better Pb-free solder alloy has been developed, new failure modes have been encountered, or test practices have been optimized.

As is shown in Figure 3.9, the development of a complete environmental test plan requires interaction between several groups. Qualification test parameters frequently accelerate the life of the Pb-free interconnections by one or multiple (safety factor) service lifetimes. The test is typically destructive and performed on a representative production sample or on lot-samples.



**Figure 3.9** Roles of acquisition personnel in environmental design/test tailoring process [Source: MIL-STD-810, Figure 1.2].

Qualification tests use assets that replicate, as much as possible, the design and manufacturing processes used to make the fielded hardware, including any pre-treatments. The tests are typically performed before the start of full production, or after a design change during production. Among the accelerated life tests are temperature cycling (TC), mechanical shock, and vibration. The typical methodology is to establish the qualification test parameters based upon a computational model, which correlates the accelerated aging test parameters to service life conditions. Qualification tests can include or be used in conjunction with accelerated life testing (ALT) or highly accelerated life testing (HALT) testing, which are arranged in such a manner that the accelerated aging test parameters only activate the service life failure modes.

### 3. Design

---

The greater the degree of acceleration in a test as compared to service, the greater the risk of applying these tests directly to Pb-free. If the qualification test is intended to verify lifetime in a specific application environment, then current test protocols are probably insufficient, and need to be reassessed in light of the new Pb-free material behavior and fatigue models. The typical test method development includes:

1. Service life determination and decomposition of environments (TC, Vibe, Shock) as defined by (or with the concurrence of) the customer.
2. A model correlating solder stress cycles to fatigue life for a particular alloy and part (created by reliability and used by the customer/test method engineer to create qualification requirements).
3. The definition of test method details to provide confidence of field performance (e.g., to verify a LRU lifetime with margin) which includes:
  - Starting condition of the LRU (e.g., ESS completed, preconditioned, newly manufactured, etc.)
  - The number of LRUs
  - Established vibration levels and durations
  - Established shock levels, pulse type and number of pulses
  - Established temperature cycling, temperature, ramp rate, dwell time
  - Established the sequence of testing (which test on which LRU)
4. Criterion for successful completion of the test (electrical performance, visual criterion, destructive physical analysis, etc.) before the test starts.
5. Execution of the test (monitoring electrical functionality, type of test equipment, calibration, etc.).
6. Review of electrical results and physical inspection.
7. Disposition of failures (if any) and retest (if necessary).
8. Certification of completion.

Depending upon the heritage of the program (DoD Service Branch, NASA, Commercial Avionics, etc.) A&D products have many current baseline practice qualification test approaches (Table 3.8).

Standard/Method/ Approach	Origin	Comments	Issues/Gaps
MIL-STD-810 Department of Defense Test Method Standard	U.S. DoD	Provides engineering direction for considering the influences that environmental stresses have on military equipment throughout all phases of its service life. Uses an environmental tailoring process that results in realistic material designs and test methods based on material system performance requirements.	SnPb assemblies have been implicitly used in its development. The document has 804 pages and the word “solder” is mentioned twice in the fluid contamination section. The methodologies are generally ok but all the set points for mechanical stress tests involving temperature cycle, vibration, or shock need to be reconsidered for Pb-free failure modes and Pb-free models are needed to validate the tailoring approach.
MIL-STD-1389 Requirements for Employing Standard Electronic Modules	U.S. DoD	This standard establishes the design requirements for Standard Electronic Modules (SEM) and includes requirements for thermal cycle, vibration, and shock.	No Pb-free material has yet proven to meet all environmental requirements per Section 5.3.
MIL-S-901 Requirements for Shock Tests, High Impact (of) Shipboard Machinery, Equipment and Systems	U.S. DoD (Navy)	The purpose of this specification is to verify the ability of shipboard equipment and installations to withstand shock loadings which may be incurred during wartime service due to the effects of nuclear or conventional weapons.	Most Pb-free materials fail simple drop shock testing. Some work is underway in evaluating low silver content materials for compliance, however thermal cycling life may be impacted.

### 3. Design

Standard/Method/ Approach	Origin	Comments	Issues/Gaps
RTCA-DO-160 Environmental Conditions and Test Procedures for Airborne Equipment (implied to electronics)	Radio Technical Commission for Aeronautics	RTCA-DO-160 is intended to provide practical boundary conditions between the requirements of the real world installations and performance of installed equipment. The document outlines a set of minimal standard environmental test conditions (categories) and corresponding test procedures for airborne equipment.	The document has 406 pages and the word solder is not mentioned in the document. RTCA-DO-160 (or its precursor, DO-138) has been used as a standard for environmental qualification testing since 1958 suggesting that SnPb acceleration factors have been implicitly used in its development. Vibration test levels/durations and shock levels/durations are specified for various aircraft types and location zones on the aircraft. These tests need to be evaluated for Pb-free solder fatigue models, aging effects on vibe/shock and failure modes.
RTCA-DO-254 Design Assurance Guidance for Airborne Electronic Hardware	Radio Technical Commission for Aeronautics	RTCA-DO-254 provides design assurance guidance for the development of airborne electronics hardware such that it safely performs its intended function, in its specified environments.	RTCA-DO-254 is a general requirement for the development of assurance plans and does not specifically mention solder alloy considerations.
GEIA-STD-0005-3 Performance Testing for Aerospace and High Performance Electronic Interconnects Containing Pb-free Solder and Finishes	AIA, GEIA, AMC	Provides a methodology for testing assemblies with Pb-free interconnections emphasizing material differences in Pb-free solders.	Combined environment test approach needs improvement. Acquisition and assessment of Pb-free field data needed to validate protocol approach.

Standard/Method/ Approach	Origin	Comments	Issues/Gaps
IPC-9701A Performance Test Methods and Qualification Requirements for Surface Mount Solder Attachments	IPC	Focuses on electronic interconnection assembly thermal cycling testing.	Addresses Pb-free in an appendix that provides an option for extended dwell time, but does not differentiate between the various Pb-free solders.

**Table 3.8 Summary of some current baseline practice qualification test approaches.**

*Issues/Gaps/Misconceptions*

1. Gap: The computational Pb-free solder joint models that are required to develop the acceleration factors needed to correlate the accelerated aging test parameters with the service life conditions, are at various states of maturity.
2. Gap: Without accurate acceleration models, the use of the current specifications may not provide sufficient margin.
3. Gap: Current tests do not consider Pb-free solder properties or failure modes during test tailoring, except GEIA-STD-0005-3.
4. Gap: A particularly challenging issue is to properly account for the order of environmental fatigue testing. For instance, performing low amplitude vibration testing on a Pb-free assembly has been shown to nearly double its life when subsequently subjected to higher vibration levels [13].
5. Gap: GEIA-STD-0005-3 suggests some protocol approaches for “performance” tests with the designer deciding on purpose and use of the results. Still, this document needs more time for user feedback in order to validate its acceptability.
6. Gap: Since there is a rapid rate of new information being accumulated for Pb-free use in A&D applications, there needs to be a way to make adjustments to the qualification requirements and/or contract costs developed during the initial project planning. Not three to five years later when the qualification of the LRU or the vehicle system is being performed.
7. Issue: Until Pb-free qualification requirements are worked out, heritage SnPb based test protocols will continue to be used at risk.

### 3. Design

---

8. Issue: LRU qualification tests typically do not consider fatigue exponents associated with the acceleration of the PCB failure mechanisms, such as copper PTH fatigue or laminate fatigue leading to pad cratering. It may not be possible to evaluate thermal cycling solder fatigue without having the PTHs fail first, because the copper fatigue exponent is considerably higher than the solder.
9. Gap: Tin whisker growth is sporadic, inconsistent, intermittent, and is sensitive to many factors, especially initial conditions. Existing whisker growth models are limited in their ability to predict whisker growth rates, latency periods, surface densities, morphologies (especially whether they grow straight or kinked), or ultimate lengths. Adequate data is unavailable for analysis, and qualification tests are usually too brief to detect whisker problems.
10. Gap: There are insufficient programmatic considerations to account for the rapid changes in Pb-free reliability knowledge. The time that transpires from the budgeted qualification test in the contract, to the time of actual performance, is typically three to five years. Thus, there is a potential for significant changes to the qualification cost and schedule.

#### *Conclusions*

While a consensus is still lacking in qualification test requirements, a Pb-free focused test methodology would better suit the A&D industry. If the qualification test is intended to define minimum integrity, then it may be sufficient.

#### *Recommendations*

Consider an approach in which qualification testing requirements are considered application specific, and consider Pb-free material properties and failure modes in the test method development. To support this course of action, several additional recommendations are presented:

1. Reassess methods and margin levels in qualification tests intended to verify lifetime in a specific application environment. This will account for the new Pb-free material behavior and fatigue models.
2. It is strongly recommended that qualification testing parameters must be based upon service life requirements, and not simply on lower bounds benchmarks, as is the case in most current qualification and acceptance documents. A computational model is the only cost-effective means to realize this goal.
3. Solicit feedback from users of GEIA-STD-0005-3 to assess strengths and weaknesses of its approach.

4. Generate a complete database of material properties and reliability data for the preferred Pb-free alloys (e.g., SAC105, SAC305, SAC405, and SnNiCu) and complete various prediction models. Note that several industry/academic consortia and working groups have embarked in such work; most notably, but not limited to, University of Maryland CALCE Electronic Products and Systems Consortium, Auburn University Center for Advanced Vehicular Electronics (CAVE<sup>3</sup>), and UNOVIS.
5. Intensive test efforts are needed which continually validate computational models against current and future package designs, including Pb-free solder joint geometries, materials sets and test, as well as service life environments.
6. Much more work is needed to understand how tin whiskers grow under various conditions.
7. Customer program and systems engineering plans should require a re-evaluation of the qualification plans prior to execution to ensure that the most up to date Pb-free reliability knowledge is considered.

#### 3.2.10 Reliability and Life Requirements

##### *Current Baseline Practice*

MIL-HDBK-217 has been a primary reference used in generating program-specific reliability requirements that has evolved with many years of SnPb assembly data. For tin whiskers, while no reliability standard exists, GEIA-STD-0005-2 provides requirements for identifying risk levels which subsequently can be utilized for mitigation plans.

Life analysis is based on an evaluation of wear out mechanisms such as solder fatigue. In the life assessment of Pb-free assemblies, the failure mechanisms (Section 7.0, Reliability) are evaluated to the extent permitted by the maturity of the models.

##### *Issues/Gaps/Misconceptions*

1. In regards to MIL-HDBK-217, the influence of Pb-free on pi factors has not been established.
2. For Pb-free solders, solder fatigue models are at various states of completion.
3. Incomplete models prevent use of tin whisker growth in the life determination.
4. Lack of long term A&D Pb-free solder use data hinders improvement of the life models.
5. There is a lack of models for the other failure modes exacerbated by Pb-free solders such as intermetallic failure, pad cratering, conductive anodic filament formation, etc.

### 3. Design

---

#### *Conclusions*

Use of MIL-HDBK-217 as a reliability standard for assemblies using Pb-free interconnections may not be accurate at this time. There are no reliability standards or life models for tin whiskers. As with SnPb solders, the fidelity of life models for failure modes other than solder fatigue could be improved.

#### *Recommendations*

1. The generation of reliability models via a physics-of-failure approach should be given more attention and considered as an alternative for a methodology.
2. GEIA-STD-0005-2 should be augmented as more failure data becomes available.
3. There is a need to obtain life data from fielded Pb-free assemblies in environments comparable to A&D applications.
4. Models need to be developed for Pb-free solder fatigue and other Pb-free failure modes.
5. Increase the use of prognostics/health monitoring methods and “on-board” environmental data recording to improve subsequent analysis of field data. These methods must be sensitive to intermittent failures of short duration.

#### **3.2.11 Cost Associated with Pb-Free Electronics**

##### *Current Baseline Practice*

The transition by the supply base to Pb-free electronics has resulted in new and increased costs to the OEMs to manage risk and maintain reliability for A&D products. These costs include, but are not limited to:

1. Preparation and governance of Pb-free Control Plans.
2. Engineering efforts to understand the technical performance of Pb-free electronics, particularly regarding reliability risk and product sustainability.
  - Cost to develop design rules and guidelines for Pb-free electronics.
  - Cost to develop reliability prediction models for new alloys, combinations of alloys, and mixtures of these with SnPb.
  - Cost to develop new test protocols.



3. Increased supply chain management efforts.
  - Cost to add new purchase order notes or drawing notes forbidding the use of Pb-free electronics without contractual approval.
  - Costs to track, analyze and mitigate the extensive numbers of piece part and assembly changes to Pb-free.
4. Increased receiving inspection activities to detect unexpected intrusions of Pb-free electronics and their disposition (Section 4.11, Manufacturing).
5. Increase in configuration management of Pb-free product and the corresponding documentation – including product identification and labeling.
6. Increase in manufacturing costs associated with Pb-free builds to include tighter process controls, mitigation strategies, and product acceptance.
7. An expected increase in frequency and cost to rework and repair defective mixed alloy electronics (containing SnPb solder and Pb-free components) and 100% Pb-free electronics – this applies to both work-in-process hardware and fielded systems.
8. An increase cost in the sustainment of dual lines within depots to accommodate SnPb and Pb-free and the configuration management of dual systems.
9. Increased awareness and product build repair and rework training.

There is also a growing impact on the procurement cost of COTS materials:

- Due to the shift in supply and demand, SnPb-based COTS component prices have increased by 30% to 50%, with the largest percentage occurring for the lowest cost components (capacitors, resistors, etc.).
- COTS components no longer available with SnPb-coated leads are being reprocessed using SnPb hot solder dipping to ensure acceptable component solderability, and a mitigation against tin whisker growth on leads coated in pure tin.
- COTS Ball Grid Arrays (BGAs) that are no longer available with SnPb solder balls are being reballed with SnPb solder balls.

As A&D companies are forced to transition to Pb-free electronics, the number and severity of technical risks have increased. The cost impact ranges from the need to train designers in the use of these new alloys, to the associated R&D and test. There is also a need for familiarity with the capital investment cost to establish new production lines that are dedicated to Pb-free manufacturing and sustainment processes.

### 3. Design

---

All of these factors increase cost and create a dilemma for program managers who are trying to maintain the appropriate balance between increased cost and reduced risk in their product deliveries.

#### *Issues/Gaps/Misconceptions*

1. Issue: COTS component suppliers are continually assessing their proportionately higher costs to produce SnPb-based products for the relatively small high-reliability, high-performance electronics market. As a result, further cost increases are expected from the shrinking number of component manufacturing companies that remain willing to continue to produce both Pb-free and SnPb-based products.
2. Issue: The need to verify the material content in COTS electronics is further aggravated by the failure of COTS suppliers to change the component part number when they make a material change. This has resulted in a new cottage industry of companies that specialize in inspection screening and reprocessing of COTS components for A&D assembly and integration companies. The reprocessing services can encompass turn-key component procurement, inspection, component hot solder dipping, BGA reballing, and kitting for the electronics assembly company. The cost of these services can become excessive relative to the Current Baseline Practice cost of a component, when the number of components to be reprocessed is small, and driven by the set-up costs and actual reprocessing time.
3. Misconception: There is a misconception that COTS components are truly “off-the-shelf.” The shrinking “off-the-shelf” availability of SnPb-based components is compelling electronics assembly companies to engage in reprocessing Pb-free components, even when SnPb-based components can be purchased. This unexpected cost scenario occurs when the component supplier agrees to sell SnPb-based components, but with a delivery lead-time quoted in excess of six to twelve months. This compels the use of reprocessed Pb-free components to meet schedule demands. A further variation on this dilemma is when a COTS supplier will sell the required SnPb-based components, but only in very large “minimum quantity buys.” Faced with the cost of producing 5,000 SnPb-based parts in order to get 50 needed parts, the reprocessing of more readily available Pb-free components is opted.
4. Issue: The reprocessing of Pb-free components has the added potential of negatively impacting the reliability of the products, which can become a cost driver for the end user.
5. Issue: Rework and repair costs are expected to increase as a result of:
  - Reduced product reliability from the use of Pb-free solders in harsh A&D operating environments, exacerbated by the random growth of tin whiskers that result in a product failure.

- The known and unknown incompatibilities of SnPb solders and a plethora of Pb-free component and surface finishes.
  - More demanding rework and repair processes to rigorously minimize and control the heat-affected zone from soldering at the higher temperatures required by Pb-free solder alloys.
  - The unrecoverable damage to a CCA that can occur when attempting to remove a conformal coating applied during production to mitigate against tin whiskers.
  - The cost of configuration management and control of mixed or Pb-free electronic products.
6. Gap: From a business perspective, crisply segregating and capturing the multiple cost impacts of Pb-free electronics is problematic at best, and becomes a cost driver itself if one wants to accurately compile the actual increases in product design, development and test, supply chain management, manufacturing, repair costs, and the imbedded impact on overhead and General and Administration (G&A) costs. Accurately predicting the total cost of the research and development required for the A&D community to transition into Pb-free electronics is a complex challenge which will be addressed in Phase II of The Lead Free Electronics Manhattan Project.
7. Issue: From a systems engineering perspective, the requirements allocation process for electronics must now include a design cost trade-off showing the impact of using Pb-free electronics, even though that impact is not completely understood, and is currently not well quantified.

#### *Conclusions*

The cost impact on the A&D industry from the commercial supplier shift to Pb-free electronics is pervasive, touching virtually all aspects of business (Table 3.9). The impact on design, manufacturing, test, and sustainment will continue to grow, perhaps stabilizing only after the A&D industry has also succumbed to the complete transition to Pb-free electronics. The full effect on product sustainment is yet to be determined, adding to the potential cost impact as the number of mixed and 100% Pb-free electronic systems enter fielded service.

3. Design

Summary of Pb-Free Electronics Cost Increases	
New Labor Costs	New Material Costs
<ul style="list-style-type: none"><li>• Prep and Implement Lead Free Control Plans</li><li>• Engineering and Manufacturing R&amp;D for Pb-Free Electronics Transition</li><li>• Added Detail to Product Design and Build Packages</li></ul>	<ul style="list-style-type: none"><li>• Reprocessing of Pb-Free Components to SnPb</li><li>• New Generation of More Costly Conformal Coatings</li><li>• New Capital Investments</li></ul>
Increased Labor Costs	Increased Material Costs
<ul style="list-style-type: none"><li>• Supply Chain Management</li><li>• Receiving Inspection</li><li>• Configuration Management</li><li>• Manufacturing and Rework</li><li>• Repair (Sustainment)</li><li>• Training</li></ul>	<ul style="list-style-type: none"><li>• SnPb-Based Components</li><li>• Scrap from Reliability Failures</li></ul>

Table 3.9 A summary of cost increases. Aerospace and defense costs to cope with Pb-free electronics include new and increased labor and material costs.

Accurately predicting and quantifying the total cost impact is perhaps more expensive than the value of the information. In short, the use of A&D Cost Accounting Standards (CAS) will ultimately link these new and increased costs to the bottom line, and will flow into pricing calculations.

The system engineer – and ultimately, the electronic designer – must include the cost impact from Pb-free electronics in their system requirement allocations and design trade spaces.

Recommendations

Recognizing that the cost growth caused by Pb-free electronics is impacting the entire A&D industry and customer community, the challenge of thoroughly understanding and accurately quantifying those costs needs to be attacked as a community. The envisioned three-year Lead Free Electronics Manhattan Project – Phase III, will focus on the research and development costs. Ancillary studies will need to be defined and funded to better understand and quantify the other cost impacts.

3.2.12 Requirements Closure

Unfortunately at this time, Pb-free solders are not consistently “as good or better” than SnPb, are less mature, have significantly different material properties, and have new failure modes that need to be considered. Pb-free risk management will influence many of the detailed requirements used in the design of electronic systems, in order to ensure reliable and safe A&D product performance.

3.3 HARDWARE DESIGN

The hardware design process begins once requirements for a program are agreed upon between the customer and the supplier. Several design elements are impacted by Pb-free (Table 3.10).

Location	Design Element	Impact
Circuit Card Assembly (CCA)	Electronic Parts	High
	Mechanical Parts	Medium - High
	Connectors	High
	Electrical Schematic	None - Low
	Mechanical Design	Low - Medium
	Materials	Medium - High
	Solder	High
	Printed Circuit Board	High
	Enclosures	Medium - High
System	Mechanical Housing	Medium - High
	Non-CCA Electrical Assemblies	Medium - High

■ A&D Low Risk   ■ A&D Low/Moderate Risk   ■ A&D Moderate/High Risk   ■ A&D High Risk

Table 3.10 Hardware design elements impacted by Pb-free.

### 3. Design

---

Elements of hardware design include electronic and mechanical parts, PCBs, interconnect materials (solder), coatings and encapsulants, connectors, enclosures, cabling, and other non-CCA hardware. This section will discuss how Pb-free influences these design elements and will provide recommendations on how to mitigate the potential risk of Pb-free technology.

#### 3.3.1 Preferred Parts List: Selecting Electronic and Mechanical Parts

##### *Current Baseline Practice*

The preferred parts list (PPL) provides hardware designers a directory of electronic and mechanical parts that have been qualified in some manner. Typically, the PPL is complemented by a preferred supplier list because there are often multiple suppliers for one electrical part (e.g. mil-spec parts). The PPL is standardized at the corporate or business unit level, and as such, the part selection process for the PPL is application and customer independent.

The current baseline practice within the A&D industry and similar markets is to increase the information obtained for each part listed in the PPL. This additional information primarily includes details on plating and soldering materials and is critical for manufacturing, reliability, and sustainment. Sources for this “new” information include manufacturers’ datasheets, manufacturers’ websites, and commercial part databases (Silicon Expert, Greensoft, IHS, and Partminer).

Information gathering should be sufficient, as restricting or requiring materials is not typically performed at the PPL, but is instead driven by customer or application requirements. However, current baseline practice within the A&D industry and similar markets is to identify alternatives to Pb-free parts (defined as parts with Pb-free tin plating or Pb-free solder attach). Particularly challenging are the cases where suppliers have changed from SnPb to Pb-free, and have not changed part number because they claim it is form-fit-function interchangeable. If the part finish or ball material is found to be unacceptable for the particular A&D application, it can sometimes be altered to refinish with SnPb (e.g., hot solder dipping, re-plating or BGA reballing) and re-identified with an internal number.

##### *Issues/Gaps/Misconceptions*

1. Many of the limitations in the current baseline practice are driven by the inadequacies of the current industry standards (Table 3.11).
2. Part suppliers have changed to Pb-free finishes without changing part numbers, significantly complicating management of parts.
3. GEIA-HB-0005-2 needs to be updated to include BGA reballing.

Industry Standard	Topic	Issues
J-STD-609	Labeling of Electronic Parts	<ul style="list-style-type: none"> <li>• Incomplete information on solder and plating</li> <li>• Does not identify surface finish plating process</li> <li>• Does not identify other environmentally-friendly materials (e.g., halogen free)</li> </ul>
J-STD-020	Moisture and Temperature Sensitivity Levels	<ul style="list-style-type: none"> <li>• Focus is on plastic encapsulated microcircuits</li> <li>• Other components (e.g., plastic capacitors, etc.) have not adopted similar standards</li> </ul>
JESD201A	Tin Whisker Acceptance Requirements	<ul style="list-style-type: none"> <li>• Based on tests not designed to demonstrate extended life in severe environments</li> <li>• Testing frequency insufficient</li> </ul>

**Table 3.11** Some Pb-free related industry standards for parts.

### Conclusions

The process of identifying, selecting, and documenting electronic and mechanical parts for insertion into a PPL, must be radically modified in response to the introduction of Pb-free electronic parts into the supply chain.

### Recommendations

The following actions are recommended for electronic parts on the PPL:

1. Additional categories must be added to the PPL database to capture all issues identified by the reliability, manufacturing, and sustainment teams (Table 3.12).
2. Parts without required information should be considered restricted for use without additional qualification or conclusive material analysis.
3. Always make direct inquiries to the part manufacturer or distributor on the availability of alternatives to Pb-free tin plating.

3. Design

- 4. Internal surface finish information should be obtained for those parts with non-encapsulated metal internal surfaces (e.g., crystals, oscillators, relays, hybrids, etc.).
- 5. Update GEIA-HB-0005-2 Section 9.

Tin-Lead Parts	Pb-Free Parts	Reason for Addition
Technology	Technology	
Electrical Ratings	Electrical Ratings	
Temperature Ratings	Temperature Ratings	
Moisture Sensitivity Level	Moisture Sensitivity Level	
Electrical Parameters	Electrical Parameters	
Package Style	Package Style	
Obsolescence	Obsolescence	
	Peak Package Body Temperature <sup>1</sup>	Manufacturing and sustainment process control
	Minimum/Recommended Peak Reflow Temperature	Manufacturing and sustainment process control
	Process Sensitivity Level <sup>2</sup>	Manufacturing and sustainment process control
	Solder Bump Material	Reliability and manufacturing and sustainment process control
	Solder Ball Material	Reliability and manufacturing and sustainment process control
	Lead Surface Finish Alloy Composition <sup>3</sup>	Reliability and manufacturing and sustainment process control; Tin whisker risk assessment



Tin-Lead Parts	Pb-Free Parts	Reason for Addition
	Lead Surface Finish Thickness <sup>3</sup>	Reliability and manufacturing and sustainment process control; Tin whisker risk assessment
	Surface Finish Plating Process (Matte, Satin, Bright) <sup>3</sup>	Tin whisker risk assessment
	Lead Underplate Alloy Composition <sup>3</sup>	Tin whisker risk assessment
	Lead Underplate Thickness <sup>3</sup>	Tin whisker risk assessment
	Lead Base Metal Alloy Composition <sup>3</sup>	Tin whisker risk assessment
	Whisker Mitigation Activity	Tin whisker risk assessment
	Lead-to-Lead Gap <sup>3</sup>	Tin whisker risk assessment
	Product Class Level Qualification for Tin Whisker Test Results (Class 1A, Class 1, Class 2, Class 3) <sup>3</sup>	Tin whisker risk assessment
	RoHS Compliance	Tin whisker risk assessment
	REACH Compliance	Compliance reporting

Table 3.12 Recommended Information for the PPL

<sup>1</sup> As defined by latest version of J-STD-020<sup>2</sup> As defined by latest version of J-STD-075<sup>3</sup> As defined by latest version of JESD201

### 3. Design

---

#### 3.3.2 Bill of Materials: Selecting Electronic and Mechanical Parts

##### *Current Baseline Practice*

Once the PPL is developed, hardware designers select parts for the CCA. The current baseline practice for creating a bill of materials (BOM) within the A&D industry and similar markets, using Pb-free electronic and mechanical parts, is to develop a part selection process flow in collaboration with manufacturing, sustainability, and reliability. In combination with the technical guidance given in GEIA-HB-0005-2 Section 9 (Table 3.12), the designer should consider:

1. Are any of the materials within the part restricted by customer or system requirements?
2. Are any of the materials within the part not compatible with the manufacturing process in regards to peak package body temperature, minimum/recommended peak reflow temperature, process sensitivity level, moisture sensitivity level, cleaning, and conformal coating?
  - Can these incompatibilities be resolved?
3. Is the part sufficiently mitigated for tin whiskering as called out by an internal LFCP defined by the latest version of GEIA-STD-0005-2?
  - If not, what mitigation practices are acceptable?
4. Is the part capable of meeting reliability requirements (lifetime, MTBF)?
  - If not, what mitigation practices are acceptable?
5. Are part finishes and ball metallurgy compatible with SnPb solder alloys?

If solder dipping or reballing is performed to resolve the issues listed above, these processes should be qualified and an internal part number should be modified to track these altered parts.

##### *Issues/Gaps/Misconceptions*

1. Issue: Designers in the A&D community will typically use heuristic rules, built up over many years, to guide the initial part selection process. Examples can include maximum component size or minimum lead pitch. These result in a more streamlined design process, but these assumptions may be dramatically incorrect for Pb-free, resulting in additional design revisions or increased risk of field failures.
2. Issue: Some designers will attempt to maintain SnPb design rules by eliminating all Pb-free materials through solder dipping or BGA reballing. However, solder dipping and BGA reballing requires additional processes to manage the risk of re-processing such as GEIA-STD-0006 (hot solder dip) and reballing (industry standard underway). One caution is that not all parts can be hot solder dipped (J-leaded parts for instance) or reballled (fine pitch BGAs with no Nickel barrier metallization).

3. Issue: In PCB design, there is a risk that heritage SnPb solder geometries will need to change, or solder stencil designs will need to change to adjust the solder volume and geometry for Pb-free solder.
4. Gap: Tin whisker mitigation by conformal coating of CCAs needs to be quantified and disseminated to the A&D community.

#### Conclusions

There is a significant risk for A&D programs that continue to rely on heuristic rules developed for SnPb for selecting or qualifying a Pb-free part for placement within a BOM.

#### Recommendations

The following actions are recommended for adding an electronic or mechanical part to a program or product-specific BOM:

1. Rules in the part selection process should be made significantly more conservative or replaced with actual tests or modeling until sufficient experience with Pb-free parts is developed.
2. The latest version of iNEMI *Recommendations on Pb-free Finishes for Components Used in High-Reliability Products* [14] should be part of the initial tin whisker risk assessment for Pb-free tin surface finishes (Table 3.13).
3. A final mitigation strategy at the program or product level should be in compliance with the latest version of GEIA-STD-0005-2.
4. The following parts should be banned, modified, or very carefully evaluated due to whisker risks, unless a non-penetrable physical barrier is present (e.g., nylon housing). Note that this tends to exclude all conformal coatings except hard polymers.
  - Zinc-chromate conversion coatings to prevent corrosion.
  - Zinc finish on connector bodies or board-mounted RF shields.
  - Pb-free tin-copper surface finish.
  - Pb-free bright tin surface finish.
  - Pb-free tin surface finish over brass or steel.
  - Pb-free tin surface finish subjected to continuous mechanical compressive stresses with no physical barrier between contacts (e.g., zero insertion force [ZIF] connectors, press in connectors).
  - Cd (Cadmium) coatings.
5. On a case by case basis, review parts on products which may already have extensive experience with some of these high risk finishes. An example of heritage tin use on a mechanical part is the tin finish specified on military wire lug terminals under compressive screw loading (e.g., MS20659 or MS25036).

### 3. Design

- 6. All parts with Pb-free solder alloys containing rare earth elements (Scandium, Yttrium, Lanthanum, Cerium, Praseodymium, Neodymium, Promethium, Samarium, Europium, Gadolinium, Terbium, Dysprosium, Holmium, Erbium, Thulium, Ytterbium, Lutetium) should be banned or modified due to tin whisker risks.
- 7. Failure rates, lifetime predictions, and availability should be re-evaluated for Pb-free parts.
- 8. New design rules for both PCB solder pad and solder stencils will need to be developed and tested to optimize solder joint reliability.

Solderable Finish	Base Material		
	Cu (7025, 194, etc.) (excluding Brass)	Low Expansion Alloy (Alloy 42, Kovar)	Ceramic (e.g., Resistors, Capacitors) No Lead-Frame
	Category	Category	Category
NiPdAu	1	1	1
NiPd	1	1	1
NiAu1	1	1	1
Hot Dipped SnAgCu	1	1	1
Matte Sn w/Nickel Underplate	2	NA	1 or 2 <sup>1</sup>
Reflowed Sn	2	2	2
Matte Sn w/Silver Underplate	2	2	2
Hot Dipped SnAg	2	2	2
Hot Dipped Sn	2	2	2
SnAg (1.5-4% Ag)	2	2	2
Matte Sn - 150 °C Anneal	2	2	2
SnBi (2-4% Bi)	2	2 <sup>2</sup>	2
Hot Dipped SnCu <sup>7</sup>	2 or 3 <sup>6</sup>	2	2
Matte SnCu - 150 °C Anneal (2% Cu)	3	3	3
Bright Tin w/Nickel Underplate	3 <sup>5</sup>	3 <sup>5</sup>	3 <sup>5</sup>

Solderable Finish	Base Material		
	Cu (7025, 194, etc.) (excluding Brass)	Low Expansion Alloy (Alloy 42, Kovar)	Ceramic (e.g., Resistors, Capacitors) No Lead-Frame
	Category	Category	Category
Matte Sn	3 <sup>4</sup>	2	3 <sup>4</sup>
Semi-Matte Sn	3 <sup>4</sup>	3 <sup>4</sup>	3 <sup>4</sup>
SnCu	3 <sup>4</sup>	3 <sup>4</sup>	3 <sup>4</sup>
Bright Tin	3 <sup>4</sup>	3 <sup>4</sup>	3 <sup>4</sup>
Ag (over Ni) <sup>3</sup>	1	1	1
AgPd (over Ni) <sup>3</sup>	1	1	1
Ag <sup>3</sup>	1	NA	1

■ Preferred finishes

■ Finishes with preferred tin whisker mitigation practices

■ Finishes with tin whisker mitigation practices that are less desirable than preferred practices

■ Finishes without tin whisker mitigation that are often not acceptable to users

■ Finishes to avoid

**Table 3.13 iNEMI Tin Whisker Risk Table**

**Category 1:** No tin whisker testing required; **Category 2:** Finish must pass tin whisker testing;

**Category 3:** Do not accept this finish in any case

<sup>1</sup> In general, tin whisker testing is required. However, users have accepted for approximately 10 years, and many will continue to accept, small discrete resistor and capacitor device components with a matte Sn over Ni finish. These devices are exceptions to the tin whisker test requirements but must meet all of the following criteria to be acceptable:

- The Sn finish shall be matte tin as specified above (see Section III, item 12).
- The Ni under layer shall be at least 80 micro inches.
- The supplier shall have data to substantiate control of its processes to minimize whisker growth (see JESD201).
- The devices must not require any lead forming or other stress creating operations after final finish.
- Tin plating thickness greater than 80 micro inches is the minimum that is acceptable.
- New component types must be similar in size and construction to previously accepted components.
- Plating of new component types must use the same plating lines, chemistries, etc. that have been previously accepted.
- New component types must pass whisker testing unless otherwise agreed to by both the user and supplier.

### 3. Design

---

---

<sup>2</sup> A number of users have restrictions on the use of SnBi finishes on alloy42 leadframes that are independent of tin whisker concerns. See Section III, item 8 for more information.

<sup>3</sup> In general, although whiskers on Ag and AgPd finishes are not considered an issue, the user group is very hesitant to accept these finishes due to a number of concerns including, but not necessarily limited to, electromigration and solderability shelf life.

<sup>4</sup> A small number of users may accept these finishes for devices with lead spacing greater than 1mm.

<sup>5</sup> Some exceptions exist where users may consider this option. See Section III, item 12 for more information.

<sup>6</sup> There is significant disagreement among users as to whether this finish is acceptable, regardless of whisker test results.

<sup>7</sup> Factors such as part geometry and solder coverage that result in thin areas of the finish may play a significant role in the tin whisker mitigation effectiveness of this finish.

#### 3.3.3 Electrical Design (Schematics)

The electrical design involves the “virtual” aspect of the circuit card assembly, absent the actual mechanical and materials components.

##### *Current Baseline Practice*

The current baseline practice within the A&D industry and similar markets is to make no changes in the architecture, heuristic rules, or qualification practices of electrical design.

##### *Issues/Gaps/Misconceptions*

There are two potential issues regarding electrical design and Pb-free.

1. Issue: Electromigration performance of SnPb solder is different from Pb-free solder. This may require a change in current being applied, if the material geometry is constrained. Note that the driver for electromigration mechanism is current density (current/area).
2. Issue: Changes in the output of failure mode and effects analysis (FMEA), failure mode, effects, and criticality analysis (FMECA). The assignment of occurrence numbers may change if the functional block or component is Pb-free.

##### *Conclusions*

The introduction of Pb-free will have minimal influence on electrical design; however there are some added items that need to be considered relative to Pb-free failure modes.

### *Recommendations*

1. If the design is at risk of electromigration, and very few are at this time, a review of existing test results and industry-accepted models is warranted to determine if the introduction of Pb-free solder increases the risk of a reduced lifetime.
2. Review occurrence numbers assigned for FMEA and FMECA and adjust if necessary for Pb-free functional blocks and components.
3. Consider the influence of intermittent shorts or opens on the systems operation.
4. Evaluate the tin whisker risk on high frequency circuits, since whiskers act as antennas and become an issue at 6 GHz (RF) and above [15].
5. Consider the effect of the tin whisker metal vapor arcing failure mode in the schematic design and parts selection, particularly in power circuits.
6. Consider the effect of whisker voltage and current conduction characteristics in the assessment of tin whisker shorting risk.

### **3.3.4 Circuit Card Assembly Design and Specification**

#### *Current Baseline Practice*

Once parts are selected and the circuit schematic is developed, mechanical designers then proceed to design and specify the CCA. The CCA includes the BOM, PCB and attachment material (typically solder), and assembly level tin whisker mitigations such as minimum spacing, conformal coating, and barriers.

Technical considerations for Pb-free risk management in circuit card assembly design are given in GEIA-HB-0005-2, Section 1.1 (Table 3.3). The current baseline practice within the A&D industry and similar markets, is to minimize changes to the physical design of the CCA when incorporating Pb-free parts, or transitioning to a Pb-free assembly. (Note that this can include feature geometries, feature spacing, part location, part orientation, number of layers, printed and circuit board size and thickness.) Pb-free risk mitigation has primarily focused on material solutions and additional qualification requirements. Material solutions have included the introduction and changes to coatings and encapsulants for whisker mitigation, and epoxy bonding/staking and underfill material for solder stress reduction. Acceptance criteria for these materials have either been added or modified, as a consideration of the specific challenges affiliated with Pb-free technology (e.g., specific thickness and coverage requirements for conformal coatings).

### 3. Design

---

CCA acceptance conforms to the latest versions of IPC-A-610 and J-STD-001, per the appropriate class level (note the majority of A&D CCAs are Class 3 or greater), with current baseline practice defining additional requirements when appropriate. The design analysis and verification test activities discussed in sections 3.4 and 3.5 are an integral part of the CCA design process, and several iterations through the design-analysis-test cycle can occur. The amount and magnitude of the test activities will depend upon the complexity of the design, and the amount of prior experience in testing similar designs.

#### *Issues/Gaps/Misconceptions*

1. Gap: The selection of coatings, encapsulants, staking compounds, and underfill can no longer be based on heritage rules developed for SnPb electronics.
2. Gap: The current versions of IPC-A-610 and J-STD-001 may not provide sufficient and necessary acceptability criteria, given the variation in Pb-free solder alloys (and possible combinations), the limited change in criteria from SnPb, and the inadequate set of relevant images for Pb-free solder joints. Some companies have developed internal standards as a stop gap until they believe the current versions of IPC-A-610 and J-STD-001 are adequate.
3. Issue: Unless specific alloys are identified, assembly soldering in accordance with J-STD-001 allows Pb-free solder alloys to be used if they meet the “objective evidence of reliability” requirement. This could result in sustainment challenges through the introduction of Pb-free alloys or other alloys which are incompatible with the repair solder alloy (e.g., SnPb, SAC, SnCuNi).
4. Utilizing heritage SnPb design rules for assembly stiffness and parts placement may not result in satisfactory vibration and shock performance of Pb-free soldered assemblies, particularly if the modules are large.
5. The effect of second and third reflows (e.g., solder melting events) on the reliability of Pb-free solder is not well understood in harsh environments.

#### *Conclusions*

While there are currently minimal changes to the current set of architectural design rules, designers should be aware of the material solutions and changes in acceptance criteria that have been validated and implemented within the A&D industry and similar products.

#### *Recommendations*

Specific design changes that CCA designers should consider include:

1. The recommendations in Sections 3.4 and 3.11.
2. Increases in the pin-to-hole ratio to improve hole fill.



3. Use of teardrop pads along the outer two rows of BGA components.
4. Reduction in maximum size for a BGA component.
5. Reduction in maximum case size for wave soldering of chip components.
6. Elimination of plated through holes as test points.
7. Review of the current version of IPC-A-610 and determine if it is sufficient for the program or product quality requirements. Develop an internal document to add or modify additional requirements.
8. Tin whisker mitigation: Selection of coatings and encapsulants for a CCA containing Pb-free technology should be driven by results of tin whisker risk assessment.
9. Evaluate the functional circuit element parts placement with respect to tin whisker risk and fault tree/FMEA/FMECA analysis.
10. Consider including provisions for assembly stiffening, underfilling, or part bonding to compensate for the reduced vibration/shock performance of the current Pb-free solder alloys. Selection of these should be driven by the results of mechanical and reliability analysis.
11. For sustainment, CCAs should be qualified to the type and number of repairs called out in the configuration management document. Qualification should include a minimum copper feature thickness (0.5 mil thickness is recommended).
12. Consider inclusion of prognostics monitoring devices on the CCA or the LRU as a means to record the service temperature, vibration and shock environments.
13. Develop improvements in prognostics monitoring devices to better record vibration and shock time history as well as data collection when the CCA/LRU power is off.
14. See printed circuit board assembly section regarding the incorporation of an assembly level “manufacturing assembly process control coupon” for destructive physical analysis of solder joints on challenging parts, solderability evaluation prior to building conformal coat coverage, cleaning effectiveness, etc.
15. In some applications, Pb-free BGAs might need to be reballed with SnPb solder. In others, consider whether Pb-free components can be soldered with SnPb solder (e.g., a “mixed metallurgy” connection).
16. Evaluate the effect of multiple reflows on thermal cycling, vibration and shock loading combinations.

### 3. Design

---

#### 3.3.5 Solder Selection

Solder is a key mechanical element within the circuit card assembly.

##### *Current Baseline Practice*

The current baseline practice within the A&D industry and similar markets is to call out the solder alloy for the assembly process in the build package, and to limit the solder choices to either standard SnPb configurations (60Sn/40Pb, 63Sn/37Pb, 62Sn/36Pb/2Ag) or alternative alloys that have an extensive history, or are well-qualified for a particular application (e.g., 90Pb10Sn for high temperature applications). The solder is specified to be compliant with the latest version of J-STD-006. Note that Pb-free 96.5Sn3.5Ag has also been used for many years on pin-through-hole designs.

##### *Issues/Gaps/Misconceptions*

1. Issue: Variation in manufacturing performance has resulted in different solder alloys being used in different assembly processes (reflow, wave, solder fountain, rework), but solder material is not always called out per manufacturing process, particularly for repair.
2. Issue: When multiple solders are used in assembly, certain combinations of solders are incompatible or have a narrow process window.
3. Gap: There are also comprehensive gaps and misconceptions regarding the relative performance of Pb-free solder compared to the more traditional SnPb solder. While there is an increasing belief that SnPb solder demonstrates superior performance in elevated stress conditions, and Pb-free solder demonstrates superior performance in more benign conditions, this can vary widely based on the following factors:
  - Pb-free alloy (SAC405, SAC0307, SAC305, SAC105, SnNiCuGe, SnAgCuBi, SnAgCuSb, etc.)
  - Component package (ball grid array, leaded, leadless)
  - Environmental stress (vibration, mechanical shock, temperature cycling)
4. Issue: Non-eutectic Pb-free alloys are not preferred because the pasty range can make manufacturing processing difficult.
5. Issue: Compatibility with SnPb repair is not defined. For instance, in the case of inadvertent mixing of Pb-free and SnPb, do these assemblies need to meet the full design life or would some level of partial life be acceptable?

##### *Conclusions*

Solder material is one of the fundamental changes in the transition to Pb-free, and must be managed proactively with the use of testing and analysis until Pb-free experience driven rules can be developed.

#### Recommendations

1. Due to a combination of insufficient experience in the industry, inadequate information on reliability under certain environments, and instability in the preferred Pb-free alloy for the electronics industry, this document will not recommend a specific Pb-free alloy. Instead, the reader is encouraged to review Table 3.14 and 3.15 for guidance on manufacturing, reliability, and sustainment issues.
2. Table 3.15 grades SnPb and Pb-free solders based on risk and experience (risk/experience) over a 1 to 5 scale, with 1 being higher risk and 5 being lower risk; Table 3.14 contains the exact definitions. As an example, tin/3% silver/0.5% copper (SAC305) is a relatively low risk for reflow assembly and benign temperature cycling, but is a higher risk for rework and mechanical shock.
3. Cells in Table 3.15 and Table 3.16 that contain no data introduce the highest degree of risk and require extensive testing and analysis before being sufficiently qualified. Users should be aware that experience influences risk. Therefore, there are few situations where the combination of high risk (1) and extensive industry experience (5), and low risk (5) and minimal experience, will exist (1).
4. In addition to using Table 3.15 and Table 3.16, it is recommended that designers be aware of the initial trends and heuristic rules developed by the industry on Pb-free solder adoption. These include:
  - SAC305 solder as currently the most common Pb-free alloy for reflow.
  - SnCuNi solders as currently the most common Pb-free alloy for wave and rework.
  - High silver SAC alloys (e.g., SAC405, SAC387, and SAC305) as being problematic for environments with drop or mechanical shock events.
  - SnAg solder as being used for many years in certain high temperature applications (under-the-hood, oil drilling), but has not been widely adopted as a Pb-free solder. However, the lack of Cu in the SnAg alloy results in increased Cu dissolution.
  - Pb-free solders without nickel subjected to continuous high temperature, greater than 100°C, could be susceptible to failure due to dissolution of copper bond pads and traces.
  - Pb-free solders without antimony subjected to continuous exposure (greater than six months) to temperatures lower than -10°C, could be at risk of tin pest (Reliability Section 7.0 and GEIA-HB-0005-2 Section 5.2). Note that antimony has some toxicity concerns.

3. Design

- Some studies have shown poorer performance of Pb-free solders in vibration compared to SnPb, but results are not consistent and more testing and analysis is necessary (Note: it is believed that much of the variation is due to inadequate control/reporting of solder stress levels, sample age, part type, cooling rate, etc.).
  - Pb-free solders alloyed with indium or zinc can be susceptible to rapid corrosion in humid environments.
5. Specifying compliance to J-STD-006 should be reviewed, as certain Pb-free solders may require agreement on additional specifications.
6. Specify the alloys that can be used when J-STD-001 is called out on the circuit card assembly data package.

Solder Alloys	Manufacturing			Use Environment				
	Reflow	Wave	Rework <sup>4</sup>	Temp Cycling Range		Vibration	Mechanical Shock	Combined
				Low <sup>1</sup>	High <sup>2</sup>			
Eutectic SnPb	5 / 5	5 / 5	5 / 5	5 / 5	5 / 5	5 / 5	5 / 5	5 / 5
SAC405	3 / 5	3 / 2	1 / 2	5 / 5	4 / 2	2 / 1	1 / 1	No Data
SAC387	4 / 5	3 / 2	1 / 2	5 / 5	4 / 2	2 / 1	1 / 1	No Data
SAC305	3 / 5	3 / 3	1 / 4	5 / 5	4 / 2	2 / 1	2 / 1	No Data
SAC0307	2 / 2	3 / 3	1 / 2	3 / 2	1 / 1	No Data	3 / 1	No Data
SAC Bi	3 / 1	3 / 1	3 / 2	5 / 2	6 / 1	No Data	No Data	No Data
SAC Sb	3 / 2	3 / 1	3 / 1	3 / 2	2 / 1	No Data	No Data	No Data
SnCu	1 / 1	1 / 3	1 / 1	No Data	No Data	No Data	No Data	No Data
SnCuNiGe	3 / 2	4 / 5	4 / 5	5 / 5	4 / 2	2 / 1	3 / 1	No Data
SnCuNiBi	3 / 1	4 / 3	4 / 3	No Data	No Data	No Data	No Data	No Data
SnBi	4 / 2	3 / 1	No Data	No Data	No Data	No Data	No Data	No Data
SnAg	2 / 3	2 / 1	1 / 2	5 / 3	5 / 3	5 / 3	5 / 3	5 / 2

Table 3.14 Common Pb-free Solder Manufacturing, Reliability Risk and Industry Experience Matrix

Risk/Experience

Risk: Does using this alloy in this situation increase the risk of defects or failure compared to SnPb?  
(5 indicates low risk, 1 indicates high risk)

*Experience: Does the industry have experience with this alloy in this situation?*

*(5 indicates extensive experience, 1 indicates minimal experience)*

<sup>A</sup> *Rework is defined as any soldering process with extended contact time (hand soldering, solder fountain, etc.).*

<sup>1</sup> *Low range temperature cycling has a maximum temperature less than 100 °C and changes in temperature less than 60 °C.*

<sup>2</sup> *High range temperature cycling has a maximum temperature greater or equal to 100 °C and changes in temperature greater than 60 °C.*

*Note: To ensure a manageable table, only the most common Pb-free assembly solders were included. Component solders, such as SAC105 and SAC125Ni, were not included.*

	SnPb	SAC 405	SAC 387	SAC 305	SAC 0307	SAC Bi	SAC Sb	SnCu	SnCu NiGe	SnCu NiBi	SnBi	SnAg
SnPb	Good	Good	Good	Good	Good	Good	Good	Good	Good	Good	Good	Good
SAC405	Possible	Good	Good	Good	Good	Good	Good	Good	Good	Good	Good	Good
SAC387	Possible	Good	Good	Good	Good	Good	Good	Good	Good	Good	Good	Good
SAC305	Possible	Good	Good	Good	Good	Good	Good	Good	Good	Good	Good	Good
SAC0307	Possible	Good	Good	Good	Good	Good	Good	Good	Good	Good	Good	Good
SAC Bi	Not	No	Good	Good	Good	Good	Good	Good	Good	Good	Good	Good
SAC Sb	Possible	No	Good	Good	Good	Good	Good	Good	Good	Good	Good	Good
SnCu	Possible	Good	Good	Good	Good	Good	Good	Good	Good	Good	Good	Good
SnCuNiGe	Possible	Good	Good	Good	Good	Good	Good	Good	Good	Good	Good	Good
SnCuNiBi	Not	No	No	No	No	Good	Good	Good	Good	Good	Good	Good
SnBi	Not	Possible	Possible	Possible	Possible	Good	Good	Good	Good	Good	Good	Good
SnAg	Possible	Good	Good	Good	Good	No	Good	Good	Good	Good	Good	Good

■ Good Compatibility   
 ■ Possible Issues   
 ■ Not Compatible   
 ■ No Data

**Table 3.15 Cross-Compatibility of SnPb and Common Pb-free Solders for Assembly and Sustainment**

### 3.3.6 Printed Circuit Board

#### Current Baseline Practice

The current baseline practice within the A&D industry and similar markets is to qualify PCBs using a test board with appropriate features. Once the PCB design and materials are qualified, the build package calls out specific laminate, solder mask, and solderability finish. Once manufacturing is initiated, lot qualification and acceptance is performed per the latest versions of IPC-A-600 and IPC-6012 with the appropriate level of preconditioning (SnPb or Pb-free). PCB design considerations are discussed in GEIA-HB-0005-2 Section 10 (Table 3.3).

### 3. Design

---

#### *Issues/Gaps/Misconceptions*

1. The potential for undetected cracking and delamination in the PCB is one of the greatest risks in a transition to a Pb-free CCA. Reliance on IPC slash sheets, especially those below 100 °C, may be insufficient to prevent latent damage.
2. Current PCB laminates in high complexity PCB configurations have inconsistent performance and is part of an active project by High Density Packaging User Group (HDPUG). Little work has been done by consumer electronics on higher cost laminate performance subjected to Pb-free process.
3. Gap: There are no Pb-free finishes that meet the same corrosion resistance, solderability, tin whisker resistance and dissolution resistance capabilities of a SnPb solder finish.
4. Gap: PCB thermal cycling coupon testing should be improved to capture the lot-to-lot variation.
5. Gap: CAF resistance coupon testing should be improved to capture the lot-to-lot variation.
6. Issue: Laminate materials suitable for Pb-free (high temperature) processing vary widely in sensitivity to moisture absorption, and their propensity for delamination or other damage during soldering. Supplier data may be incomplete or questionable. Rates of moisture uptake and moisture release during bake operations can be influenced substantially by the PCB design, including board thickness and distribution ratio of dielectric to copper in any of the power, ground, or signal layers.
7. Issue: Laminate properties have been known to vary from published data. Variation may be between manufacturing sites (especially offshore), or even from lot to lot. Users may consider auditing to IPC-1730 and IPC-1731.
8. Material supplier claims that a PCB material is Pb-free compatible are insufficient and the material must be evaluated in the application to determine suitability.
9. There are no standard rules for converting existing SnPb designs to Pb-free solder.
10. Issue: Unlike SnPb finishes, pre-baking Pb-free finishes prior to soldering to reduce PCB moisture content, can be detrimental to the solderability of most of the current Pb-free finishes, unless performed in an inert environment.

#### *Conclusions*

Latent damage to PCBs is one of the greatest risks in the transition to Pb-free CCAs. Mitigation of these risks can be accomplished through appropriate material selection, awareness of industry-developed heuristic rules, and rigorous product and lot qualification procedures.

#### Recommendations

Appropriate risk mitigation procedures for PCB and Pb-free can be divided between solderability plating, material selection, acceptance criteria, and handling:

##### 1. Solderability Plating

- Electroless nickel/immersion gold (ENIG) is not recommended for use with Pb-free solder due to the elevated risk of solder fracture during post-reflow handling. If used, appropriate risk evaluation should be performed.
- All PCB features with immersion tin plating should be coated with solder during assembly to prevent tin whiskers.
- All PCB features with immersion silver plating should be non-solder mask defined (NSMD) to mitigate the risk of creep corrosion.

##### 2. Develop a Pb-free PCB finish that exhibits comparable corrosion resistance to SnPb, does not whisker or tarnish, and retains long term solderability.

##### 3. Laminate Material

- Table 3.16 should be used as a reference guide for the selection of appropriate laminate material for Pb-free assembly.
- Laminator and PCB supplier chains regarding Pb-free process capability for complex PCBs are highly suspect and require independent verification.
- Thick boards (>93 mil) with elevated peak reflow temperatures (>250°C) should be built with laminate with <3% z-axis expansion between 50-260°C and <0.15 weight percent moisture absorption.
- Time to delamination (IPC-TM-650, 2.4.24.1) should be specified as T-280 of 5-10 minutes or T-288 of 3-6 minutes.
- Temperature of decomposition (IPC-TM-650, 2.3.40) should be specified at a minimum of 320°C.
- In addition to watching the PCB supplier, it is recommended that the laminator be audited and monitored by the PCB supplier using IPC-1730 and 1731, with follow up audits by the OEM customer to assure this is effective.

##### 4. Acceptance Criteria

Use simulated reflow instead of solder shock for lot qualification. A new IPC-TM-650 Test Method 2.6.27 was just issued to describe the reflow test for both SnPb and Pb-free applications covering Thermal Stress, and Convection Reflow Assembly Simulation.

### 3. Design

The IPC is currently embedding this test method into its requirements as an option that can be called out on the PCB drawing when necessary. The IPC is just starting to write a guideline document to provide more information on the use of this test method.

5. Handling
- All PCBs should be packed in moisture proof bags. (Note: IPC-1601 is in development, which will cover PCB storage and handling.)
6. Supplemental Coupons (each board lot)
- The following supplemental coupons should be considered to enhance control of the Pb-free PCB reliability and subsequent circuit card assembly quality:
- Thermal cycling coupon to evaluate plated through hole (PTH) and interconnect reliability

• CAF test coupon

• Manufacturing assembly process control coupon (challenging parts, soldering quality, conformal coat, cleaning effectiveness, rework, Cu dissolution, etc.)

Board Thickness	Peak Reflow Temperature (Forced Air Convection)	
	240 °C to Low 250 °C	Mid 250 °C to 260 °C
≤60mil	Tg140 Dicy All HF materials	Tg150 Dicy HF – middle and high Tg
60-73mil	Tg150 Dicy All HF materials	Tg170 Dicy HF – middle and high Tg
73-93mil	Tg170 Dicy HF – middle and high Tg	Tg150 Phenolic + Filler HF – middle and high Tg
93-120mil	Tg150 Phenolic + Filler HF – middle and high Tg	Tg170 Phenolic HF – middle and high Tg
121-160mil	Tg170 Phenolic HF – high Tg	Tg170 Phenolic + Filler HF – high Tg
≥161mil	Tg170 Phenolic + Filler HF – TBD	TBD

Table 3.16 PCB Material Selection Guide for Pb-Free Assembly

1. Copper thickness = 2 oz should use material listed in column mid 250 °C to 260 °C
2. Copper thickness ≥ 3 oz should use Phenolic base material or high Tg halogen free materials only
3. Twice lamination product should use Phenolic material or high Tg halogen free materials only (includes high density interconnects (HDI))



7. Develop a task list for the conversion of an existing A&D SnPb assembly to Pb-free. This activity will require a risk assessment of the existing design. For instance, an older design could simply change parts to Pb-free solder equivalents, change to a Pb-free solder laminate and PCB finish, and assemble with Pb-free solder to determine if the older design is sufficiently robust. More modern designs might need additional work for tin-whisker mitigation and solder joint geometry to make them compatible. Of course any changes would need to be validated with life testing. If older designs could change, then there might be a cost benefit since Pb-free parts could be used and A&D manufacturers would not have to completely redesign products that already perform well.

### 3.3.7 Chassis/Enclosure/COTS Mechanical Parts/Custom Mechanical Parts

Mechanical housings are designed to hold and protect circuit card assemblies from external environments, such as handling, impact, vibration, electromagnetic radiation, and corrosive elements.

#### *Current Baseline Practice*

The current baseline practice within the A&D industry and similar markets, in regard to chassis and enclosures, is to identify the surface plating or treatments for corrosion protection and ensure that it is effectively risk mitigated for tin and zinc whiskers. Mitigations include:

- Using tin plating with greater than or equal to 3wt% lead.
- Not using zinc plating.
- Only using tin plating with less than 3wt% lead in areas that will be coated with solder during assembly.
- Following the guidelines in GEIA-STD-0005-2.

#### *Issues/Gaps/Misconceptions*

1. Issue: The primary misconception regarding COTS chassis, enclosures, and parts is being aware that manufacturers could change surface finish materials without communication to the end customer.
2. Issue: Heritage finishes called out on custom mechanical parts are becoming more difficult to obtain (increased cost and lead-time).
3. Issue: Tin plated mechanical parts can have very large surface areas and be a source for very large numbers of whiskers.
4. Issue: There are many Mil-spec parts that have used pure tin, and have been used for decades, such as heritage tin used on military wire lug terminals, under compressive screw loading (e.g., MS20659 or MS25036).

### 3. Design

---

#### *Conclusions*

A significant percentage of tin whisker field failures can be traced back to surface finishes on the various elements of mechanical housings or mechanical parts. Following current baseline practice is necessary and should be sufficient to prevent future failures.

#### *Recommendations*

1. It is recommended that designers conform to current baseline practice in regard to Pb-free chassis, enclosures, and other mechanical items.
2. When designing, strive to minimize tin area in the design of mechanical items where possible.
3. Chassis designs may need to be modified to reduce vibration and shock loads transmitted to the CCA solder joints.

#### **3.3.8 Other Electrical Assemblies**

This section covers electrical assemblies that are not circuit card assemblies, such as cable assemblies, relays, filter assemblies, radar, power assemblies, and bus bars. While these assemblies do not contain PCBs, they do contain surface finishes and solders that may change during the transition to Pb-free.

#### *Current Baseline Practice*

The current baseline practice within the A&D industry and similar markets is to treat non-CCA electrical assemblies in a similar manner to CCAs where relevant. This includes identifying and mitigating surface finishes per GEIA-STD-0005-2, and proactively managing Pb-free solder alloys with the use of testing and analysis, until rules can be developed.

#### *Issues/Gaps/Misconceptions*

1. Misconception: The primary misconception regarding non-CCA electrical assemblies is being aware that manufacturers could change surface finish materials and solder without communication to the end customer.
2. Misconception: Assemblies with higher voltage and power (power input and output circuits) with finishes can be susceptible to metal vapor arcing even at sea level [16], but the design parameters are not well understood.

### *Conclusions*

Following current baseline practice is necessary and should be sufficient to prevent future failures.

### *Recommendations*

1. Recommendations outlined in sections 3.3.1 and 3.3.2 for surface finishes and 3.3.5 for solder material should be followed.
2. Increased research in metal vapor arcing is needed to establish design rules for material, voltage, coating and spacing.

## 3.4 DESIGN VERIFICATION/VALIDATION

### **3.4.1 Design for Manufacturing**

#### *Current Baseline Practice*

Design for Manufacturing (DFM) currently is an established best practice to ensure that a product can be manufactured as well as reworked/repared. Pb-free soldered assemblies can have greater variability especially if occurring in a high mix/low volume manufacturing setting. Typically rework considerations factored into this review will facilitate subsequent repair activities during sustainment.

#### *Issues/Gaps/Misconceptions*

1. Gap: Rules of thumb for manufacturability and rework/repair must be re-examined for Pb-free solder to ensure that manufacturing process variation is minimized.
2. Gap: Robustness of PCB finishes, solderability, surface conductors, PTH reliability, and laminate integrity, are often not evaluated in the context of manufacturing rework, where five to ten year old assemblies are being repaired as part of the sustainment process.
3. Gap: The rework assessment performed during manufacturing may not consider the ramifications of how to sustain an assembly being repaired five to ten years down the line.

### *Conclusions*

DFM is an established process. For Pb-free assemblies, DFM (and repair) has become more important because of the decrease in manufacturing process windows and increased variability of Pb-free processes.

### 3. Design

---

#### *Recommendations*

Continue using DFM practices to ensure that reliability and repairability objectives continue to be met. Specific recommendations for Pb-free solder include:

1. Include active involvement in product development teams by representatives of parts engineering, CCA (module) engineering, and supply chain to work specific concerns with respect to SnPb availability, Pb-free assembly as needed, Pb-free repair (including mixed technology), and Pb-free rework.
2. Leverage the use of GEIA-HB-0005-3 in the DFM process.
3. Evaluate robustness of PCB finish solderability, robustness of surface conductors, PTH reliability and laminate integrity.

#### **3.4.2 Fault Tree, FMEA and FMECA Analysis**

##### *Current Baseline Practice*

Currently Fault Tree, FMEA, and FMECA Analysis generally follows the preliminary schematic and parts list, and is typically verified through the design review processes (e.g., critical design review). These reviews are iterative and occur both internally within the design community and externally with the customer. Design practices and reviews often use checklists as part of the review process that have been derived over many years to capture lessons learned and best practices.

##### *Issues/Gaps/Misconceptions*

1. Gap: A significant gap exists in the A&D industry design practices and review checklists. Many are in various states of maturity and implementation regarding Pb-free, while concurrently, complete Pb-free designs are being done today.
2. Gap: COTS defined designs before 2006 may have changed from SnPb to Pb-free solder without notice and may impact fault analysis.

##### *Conclusions*

The fault tree and FMEA/FMECA review process is well established for many programs and the fundamental method of analysis is unchanged for Pb-free. There are expected to be greater incidence of short circuit, open circuit, and intermittent connections especially during the early introduction of Pb-free interconnect technologies.

### *Recommendations*

The following items are recommended:

1. Update design review checklist items to include Pb-free considerations pertaining to Fault tree, FMEA and FMECA Analysis.
2. Re-evaluate Pb-free COTS risks in the fault tree with particular attention on Pb-free COTS power supplies.

### **3.4.3 Electrical Analysis**

#### *Current Baseline Practice*

Currently, electrical design rules and analysis verification have not been uniformly assessed with regard to Pb-free solder and finish considerations.

#### *Issues/Gaps/Misconceptions*

The following areas are considered gaps:

1. Issue: The electrical design community has not been made aware of specific design constraints/considerations needed for Pb-free solder use in A&D applications.
2. Issue: Tin whiskers can impact circuit performance of high frequency RF circuits [15].
3. Gap: There are no current density rules established to avoid electromigration in Pb-free solder assembly.
4. Gap: The design rules for metal vapor arcing initiated from whisker shorts do not exist.
5. Gap: Although increasing data on whisker shorting voltages and currents is becoming available, it is unclear how these would impact circuit schematic design.
6. Gap: At the present time, electrical design does not provide guidance regarding physical separation between critical devices (e.g., components from different critical functional elements) to eliminate whisker risk. Physical separation between critical devices is an important analysis that requires considerable effort at the present time.

#### *Conclusions*

There remain several technical unknowns with regard to Pb-free that may affect electrical design practices in A&D applications.

### 3. Design

---

#### *Recommendations*

The following items are recommended:

1. Establish a research test and analysis plan to identify and characterize specific design constraints/considerations needed for Pb-free solder use in A&D applications such as:
  - Tin whiskers impact on high frequency RF circuits.
  - Current density rules established to avoid electromigration in Pb-free solder assembly.
  - Designing for metal vapor arcing initiated from whisker shorts.
2. Develop a method to automate critical physical part separation distance analysis.

#### **3.4.4 Solder Fatigue and Interconnect Reliability Analysis**

This section covers component types such as BGAs, micro-BGAs, Area Arrays, Leaded, Leadless, Chip Parts, and Pin-Through-Hole. Design rules of thumb for A&D Pb-free products have not yet been developed but would greatly benefit designers looking for guidance in this area. This section is comprised of some overall comments followed by a detailed discussion of vibration, shock and thermomechanical fatigue, and combined thermal and mechanical dynamic loading environments.

#### *Current Baseline Practice*

Perform fatigue stress calculations separately for each environment, (thermal cycling, vibration, shock) and determine through a linear summation of the fraction of damage, from the individual environments, if the overall program requirements are met.

#### *Issues/Gaps/Misconceptions*

Several high-level issues and gaps have arisen.

1. The fatigue resulting from stresses due to the individual environments, thermal cycling, vibration, and shock cannot be added in a linear manner using Miners law.
2. The heritage SnPb design guidelines do not adequately capture the pad cratering and intermetallic failure modes encountered in Pb-free assemblies (Figure 3.10).
3. Using SnPb solder stress design levels for Pb-free designs will not necessarily result in satisfactory life in high stress environments.

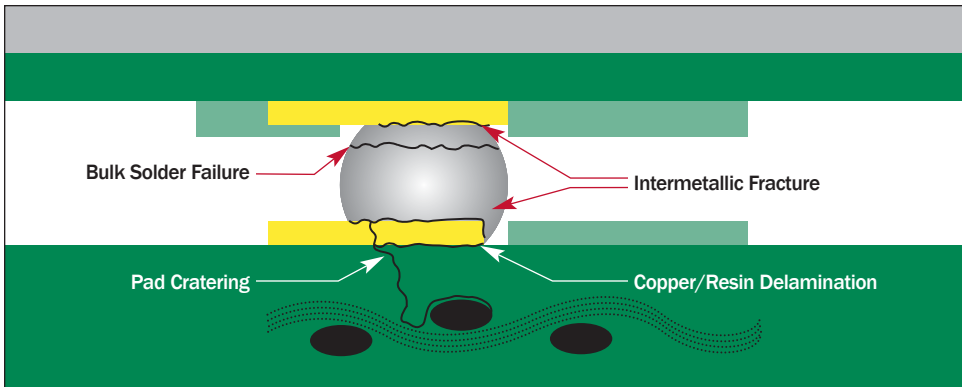


Figure 3.10 Pb-free solder interconnection failure under isothermal loading (cyclic or overstress) [2].

### Conclusions

At a high level, the over-arching solder stress analytical conclusion is that global mechanical solder fatigue analysis, used to determine solder stress levels, will not change significantly. However, the local allowable solder stress calculations will change due to (1) greater changes in Pb-free solder properties throughout its life, (2) different failure modes introduced by Pb-free solder, and (3) lower reliability level of Pb-free soldered assemblies compared to the equivalent SnPb assembly in vibration and shock.

### Recommendations

1. The Pb-free design stress levels will need to be reduced for high stress applications.
2. Further evaluation is needed so that combinations of thermal cycling, vibration, and shock stresses can be quantified for Pb-free solder.
3. The path forward will require development of new rules of thumb for global stress levels for use in the preliminary design phase to ensure subsequent detailed stresses are computed. This will ensure a minimum of design changes when the detailed interconnect stresses are analyzed.

The subsequent sections discuss each of the load types in more detail.

### 3. Design

---

#### Vibration Loading

##### *Current Baseline Practice*

Vibration can occur in many A&D conditions, especially in airborne and certain submarine environments (Figure 3.11). Global analysis remains unchanged for the assembly. A vibration reduction technique may be needed to utilize Pb-free soldered assemblies in A&D applications.



*Figure 3.11 Helicopter service conditions are very vibration intensive.*

##### *Issues/Gaps/Misconceptions*

1. Gap: In contrast to thermal cycling, vibration tested Pb-free soldered assemblies are not as reliable as SnPb assemblies for equivalent stress levels, particularly if the levels are high (Figure 3.12).
2. Gap: Vibration fatigue data for low stress conditions is lacking.
3. Gap: The effect of solder aging on fatigue behavior is unknown.



4. Gap: Generally there appears to be a complete break-down of Miner's rule. Exposing an assembly to low level vibration significantly improves subsequent vibration fatigue at high levels (Figure 3.13). While this may sound good, the opposite has not been tested, but it may be possible that very few cycles of high vibration could dramatically reduce long term low level vibration performance. In addition, the effect of vibration on subsequent thermal cycling is also not understood.

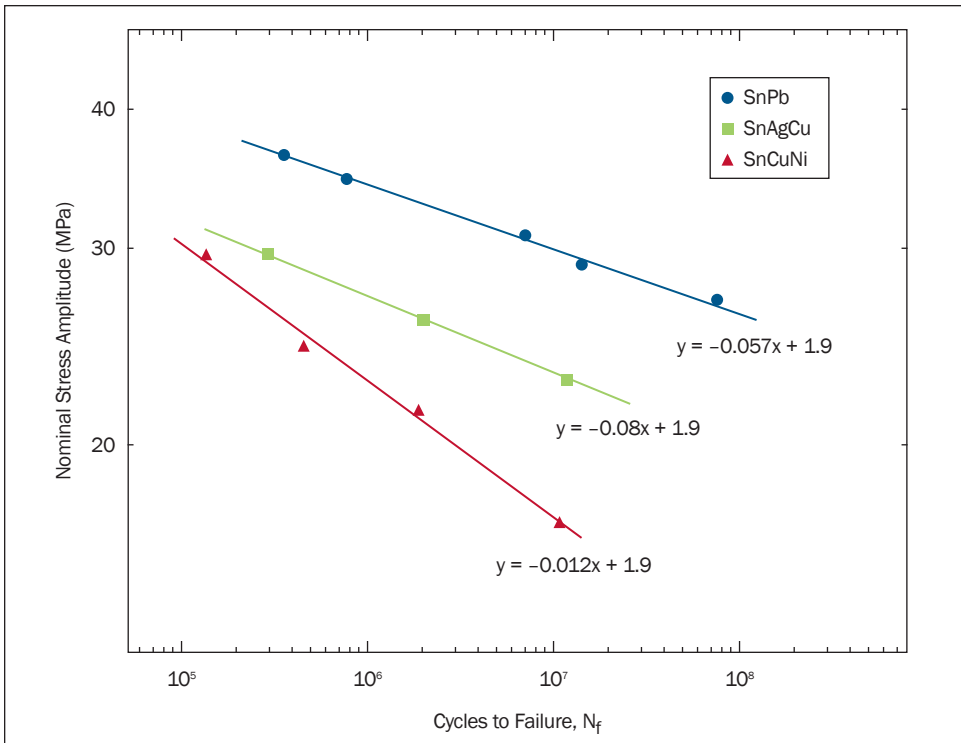
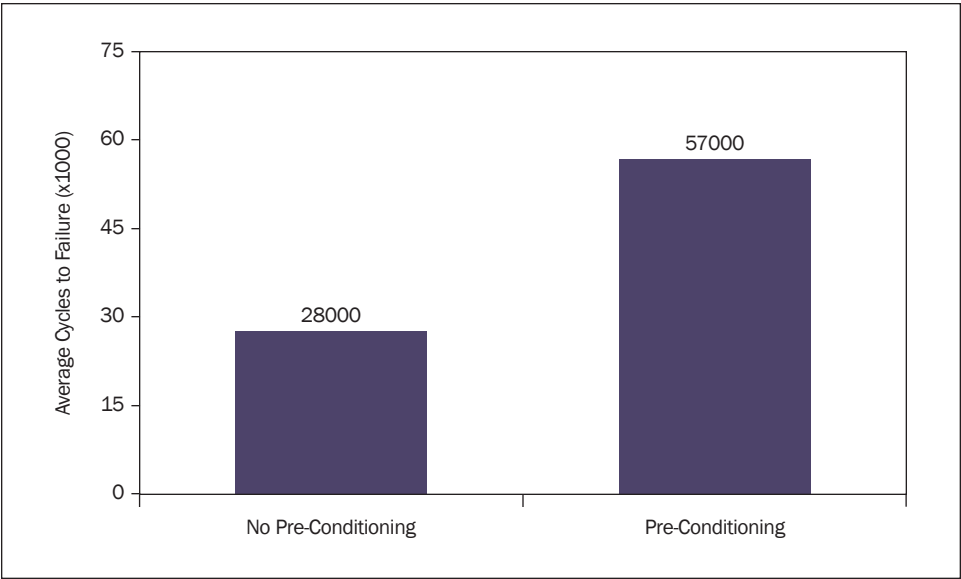


Figure 3.12 Vibration fatigue of SnPb, SAC305 and SN100C (Sn0.7Cu0.05Ni+Ge). SnPb solder exhibited greater vibration performance [17].

### 3. Design

---



*Figure 3.13 Number of cycles to solder failure for BGAs in 20G vibration without preconditioning (left) and after 220,000 cycles of 5G vibration (right) [2].*

#### Conclusions

Vibration is an environment that differentiates A&D products from consumer electronics. The vibration test which typically results in high cycle solder fatigue; but this is not always the case. Under high vibration loading, intermetallic and pad cratering failure modes can be observed in addition to solder fatigue.

#### Recommendations

1. Develop projects to define the vibration solder fatigue and interconnect reliability parameter space. In particular, develop a relationship beyond Miner's rule that can be used by designers to combine different levels of vibration, shock and thermal cycling.
2. Leverage results of this research to either validate and/or update GEIA-HB-0005-4 [18].

### Mechanical Shock Loading

#### Current Baseline Practice

Shock manifests itself in many forms in an A&D environment. Explosive shock (pyro-shock), functional shock (e.g., carrier catapults), and drop (handling miscues) shock are a few examples, shown in Figure 3.14. A considerable amount of recent work has been done in consumer

electronics products in response to cell phone drop shock failures. As a result of these drop test failures, there has been a resurgence in solder alloy changes in order to find an alloy with greater shock resistance (Figure 3.15) [19].

A.



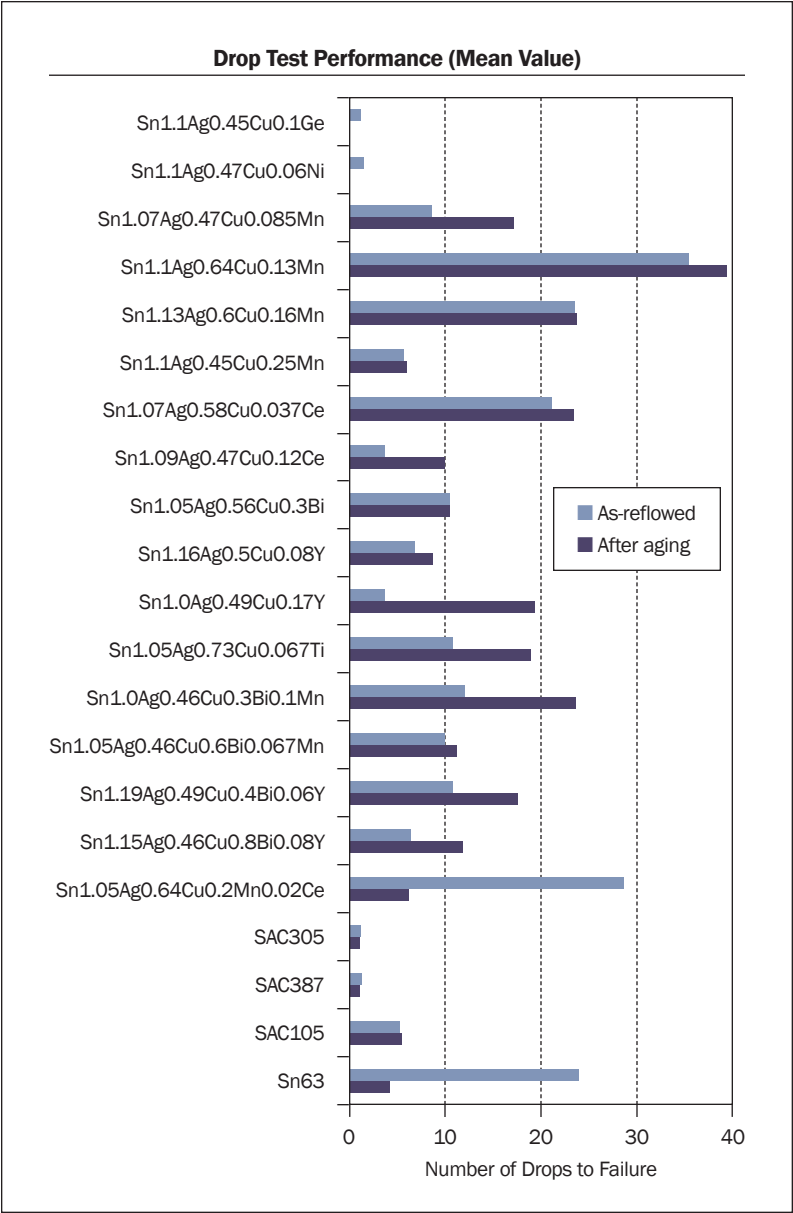
B.



*Figure 3.14 Mechanical shock manifests itself in several ways; image A., top, is an example of explosive shock while functional shock – as in aircraft carrier catapults – is shown in B., directly above.*

3. Design

A.



B.

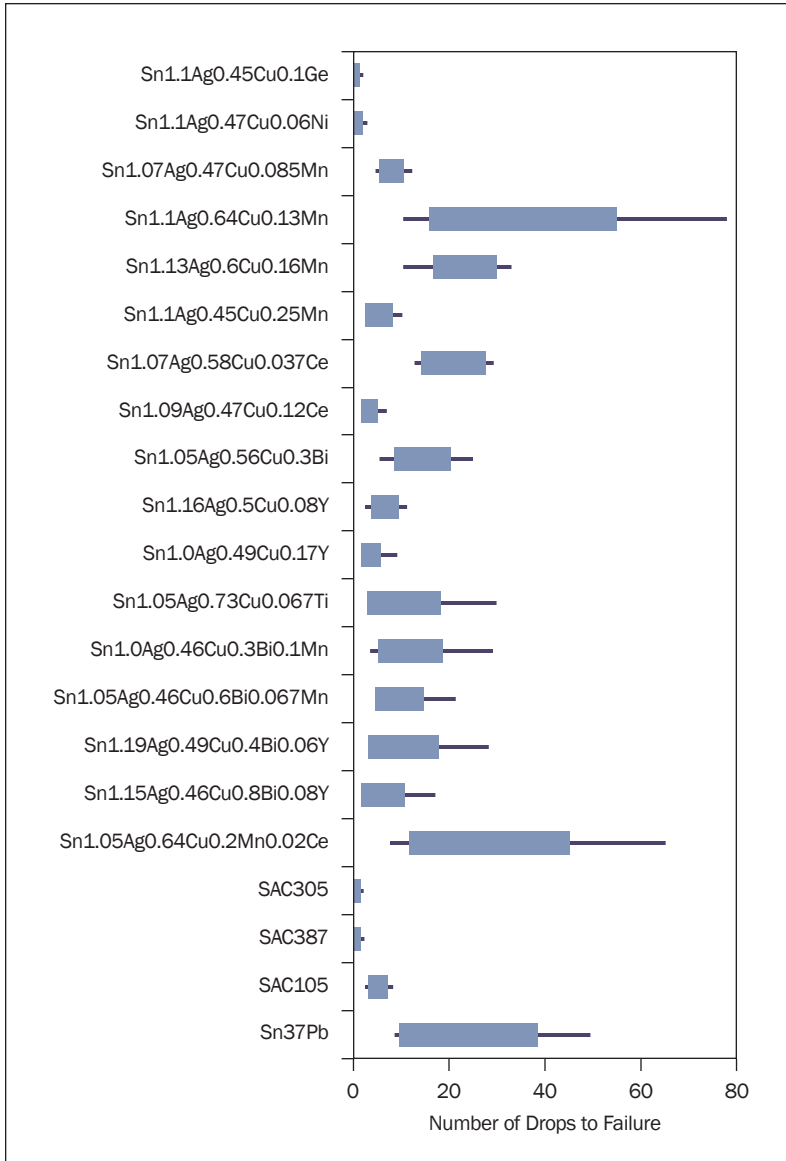


Figure 3.15 Drop tests of various Pb-free alloys compared with SnPb. (A) Drop test results after aging at 150 °C for four weeks [19]. (B) Samples were in the as-reflowed condition.

### 3. Design

---

#### *Issues/Gaps/Misconceptions*

1. Issue: The next generation of improved shock solder alloys may be comprised of many as four to five element mixtures where the additional alloy additions (as low as 0.05% by weight) can have an appreciable effect on the performance.
2. Gap: The thermal cycling data has not been done on many of these new alloys.
3. Gap: The sensitivity of the weight percentages on the alloy additions reliability has not been evaluated.
4. Gap: No data exists for MIL-STD-883C pyro-shock loading of Pb-free assemblies.
5. Gap: The role of assembly aging on shock performance is poorly understood.
6. Gap: Design rules to prevent pad cratering have been empirically derived for select alloy/PCB laminate combinations with the majority of combinations not having any design guidelines.
7. Gap: These improved shock resistant alloys are not part of J-STD-006.

#### *Conclusions*

Shock stresses are a rapid loading event that typically results in a pad cratering or intermetallic failure mode, rather than a solder failure. In addition, leverage the results of this research to either validate and/or update GEIA-HB-0005-4 (due for release in 2009).

#### *Recommendations*

1. Conduct research to determine the design stress rules for shock loading for intermetallic, pad cratering and solder failure modes.
2. Leverage results of this research to either validate or upgrade GEIA-STD-0005-3 and GEIA-HB-0005-4.
3. Evaluate these new alloys in the other A&D environments (thermal cycling, vibration, humidity, corrosion, etc.).

#### Thermo-Mechanical Loading

##### *Current Baseline Practice*

Thermo-mechanical loading (e.g., thermal shock and thermal cycling) occurs in almost every service condition for A&D equipment. The range of temperature extremes (mean temperature range), rate of temperature change (ramp rate), the exposure time (dwell) and number of exposures (cycles) will vary with the local environment. However, it is the combination of all of these parameters that will determine the amount of fatigue experienced by the product.

Developed by several industrial and academic groups, thermal cycling has been the focus of the majority of consumer electronics researchers and thermal cycling fatigue models. The University of Maryland CALCE continues to perform research on Pb-free alloys leading to the update of its models for circuit card assembly reliability. Likewise, Auburn University's Center for Advanced Vehicular Electronics (CAVE<sup>3</sup>) is doing similar work with additional focus on aging effects. MIL-STD-217 is also being utilized. GEIA-STD-0005-3, while not a reliability or reliability test standard, does provide guidance on key concerns when designing a test, albeit for reliability prediction purposes.

##### *Issues/Gaps/Misconceptions*

1. Gap: The properties of Pb-free solder change during thermal cycling, and should be accounted for during modeling.
2. Gap: The role of dwell time and ramp-rate are poorly represented in current modeling.

##### *Conclusions*

For low interconnection (joint) stresses, solder fatigue is the dominant failure mode and the fatigue performance of a Pb-free soldered assembly is greater than SnPb. As solder stress increases, SnPb is more reliable than Pb-free. In addition, leverage results of this research to either validate and/or update GEIA-HB-0005-4 (due for release in 2009).

##### *Recommendations*

1. Thermal cycling research needs to be performed on the new Pb-free solders being developed to improve the shock performance.
2. Perform research to develop design parameters for mixtures of Pb-free alloys, or mixtures of Pb-free and SnPb alloys.

### 3. Design

---

#### Combined Thermo-Mechanical and Dynamic Loading

##### *Current Baseline Practice*

The concept of combined environment has been a focused discussion for several years as the service conditions of A&D equipment tend to experience a multitude of environmental loads (e.g., thermal, vibration, shock, and others). Understanding the load types and sequences experienced by fighter jets, rockets, and missiles, for example, would provide a more accurate assessment of overall reliability (Figure 3.16).

Presently, Miner's rule of cumulative linear fatigue life has been applied for the various alloys. A notional view of cumulative damage has been presented in GEIA-STD-0005-3.



*Figure 3.16 Fighter jets and rockets can experience multiple loadings, not necessarily in sequence.*



#### *Issues/Gaps/Misconceptions*

1. Gap: The drastic change in microstructure and other constitutive material properties of Pb-free alloys, strongly suggest that linear cumulative damage theories like Miner's Rule, for multiple loadings, will not produce accurate assessments.
2. As discussed in the previous vibration section, generally there appears to be a complete break-down of Miner's rule. The effect of vibration on subsequent thermal cycling is also not understood.

#### *Conclusions*

While combined thermal cycling and mechanical loading is not well understood for SnPb solder, the field heritage suggests that the present approach of testing thermal cycling, vibration and shock independently, and using Miner's rule to combine fatigue lives for various types of loading, appears to be sufficient in many cases. With Pb-free solder there is no heritage experience to draw upon and there are indications the Miner's rule is not appropriate. Therefore, models need to be created for combined environment fatigue modeling.

#### *Recommendations*

1. Conduct both fundamental and application specific research on solder and electronic assemblies in order to develop a combined environment reliability model.
2. Develop design rules for combined environment (even if they are initially conservative).
3. Develop a qualification or reliability test to evaluate what could be considered a worst case condition for the combined environmental loading. This will reduce the risk of escapes into the field.

### **3.4.5 Product Development Testing**

#### *Current Baseline Practice*

Product development testing is presently performed per program-specific or company-specific procedures. Product development testing includes tests to assess various design requirements on product proto-types or pre-determined sub-units (e.g., CCAs or sub-assemblies). Testing can also be performed on parts, materials, or mechanical components when specific electrical/mechanical properties are of interest. Often long term accelerated life testing (ALT) in conjunction with predictive life models is performed on generic circuit card assemblies to develop failure data for a particular solder, part set, and manufacturing method.

### 3. Design

---

Finally, testing may be performed on actual production line removable units (LRUs) to identify weaknesses in the product design, as a feedback to the design optimization process. LRU testing may also be used to assess performance beyond design limits, using highly accelerated life testing (HALT) and highly accelerated stress testing (HAST). Although, it is often difficult if not impossible to correlate the results of HAST and HALT to design life, they are often effective in identifying product design weaknesses and can be used as feedback to optimize the design.

#### *Issues/Gaps/Misconceptions*

1. Issue: With Pb-free, the test method is impacted by the type of Pb-free alloy, but this information is typically not coordinated between the customer, systems engineering, hardware design, manufacturing, and sustainment.
2. Gap: There is insufficient data to establish acceleration factors between accelerated aging tests (temperature cycling, mechanical shock, vibration, and combined environments) and service life environments for Pb-free solder interconnections.
3. Gap: There is the need for a high fidelity computational solder fatigue model, which can predict fatigue of Pb-free interconnections, in order to establish acceleration factors between accelerated aging test parameters and service life conditions. This capability is required to establish qualification and acceptance test regimens.
4. Gap: There is also a need for high fidelity PCB fatigue models that can predict laminate, surface trace, inner trace and PTH failures.
5. Gap: Solder and PCB material properties (mechanical and physical) are needed to provide input parameters for first-level validation data to the computational models.
6. Gap: Rigorous HAST and HALT testing methodologies are needed, which can confidently determine the overall (HAST) design limits of Pb-free solder joints, for a particular service lifetime (HALT), including the identification of relevant failure modes.
7. Misconception: It is a misconception to assume that it is possible to design product with Pb-free interconnections based upon such generalizations as "Pb-free solder joints are more/less reliable than Sn-Pb solder joints."
8. Gap: There is a need for rigorous HAST testing methods that can identify the suspect failure modes of Pb-free solder interconnections.

#### *Conclusions*

1. Computational models are critically needed in order to develop test parameters that are based upon service lifetime requirements, thus avoiding either under design or over design of the Pb-free solder interconnections.

2. The HAST and HALT test methods are important tools in determining the design limits of Pb-free solder joints, particularly, with respect to identifying existing and new failure modes. The inclusion of these test methods must be an integral step in the Pb-free solder joint reliability assessment.
3. The definition of qualification and acceptance testing parameters must be based upon the expressed service life requirements. The computational model can provide the cost-effective means to achieve this objective.

#### *Recommendations*

1. The solder alloy and its model parameters must be agreed upon between the customer, systems engineers, hardware designers, manufacturers, and sustainment engineers so that proper mechanical test methods can be developed.
2. Establish a correlation between accelerated aging test parameters and service life conditions. Computational models are required to develop the acceleration factors needed to correlate the accelerated aging test parameters, with the service life conditions expected for Pb-free solder joints. Requirements: (a) Develop a suitable Pb-free computational model; (b) obtain material physical and mechanical properties as input data for the model, as well as to support the first-level validation of the model; and (c) perform limited Pb-free test vehicle (CCA) accelerated aging tests for final validation of the model predictions.
3. Design validation test methodology: First, the HAST on the LRU or CCA is used to identify weaknesses in the product design as a feedback to the design optimization process. Particular attention should be paid to Pb-free interconnection (bulk solder and intermetallic), PCB, and part failures. Extreme test levels are used for temperature cycling, including the use of temperature shock, as well as mechanical shock and vibration parameters. Other custom test regiments can be added, as well. Requirements: (a) Determine all “practical” failure modes in the design, with particular attention paid to those of the Pb-free interconnections, PCB, and parts. (b) Confirm that other failure modes do not obstruct the testing of the Pb-free solder joint performance and/or failure mode assessment.
4. Design verification test methodology: Once the design changes have been made after HAST, accelerated life test or highly accelerated life test is then used to determine the functional limits of the Pb-free interconnections, with respect to the service lifetime. Other custom tests can be added. Accelerated aging parameters are now correlated to the service life conditions, assuring similar failure modes. Requirements: (a) Targeting specifically the Pb-free interconnections, design limits must be determined based on service life conditions to establish the accelerated aging parameters that are appropriate for qualification and acceptance tests. (b) Confirm that the same failure modes of the Pb-free interconnection degradation prevail under both accelerated aging and service life aging processes.

### 3. Design

---

---

5. Execute an awareness campaign to emphasize the need for Pb-free material and constitutive property data, as part of an accurate product development test process. Consider this as a possible update to GEIA-STD-0005-3.
6. It is recommended that the number of test articles be increased so that an improved degree of statistical significance can be derived from failures that are encountered due to high mix/low volume manufacturing.
7. Appropriate HAST test methods and parameters must be developed to effectively determine the design limits of Pb-free solder joints, particularly, with respect to identifying relevant failure modes, and to assure that unwanted failure modes do not obscure the solder joint performance evaluation.

#### 3.4.6 Design Review

##### *Current Baseline Practice*

Key to the success of the design review process is a series of checkpoints or design reviews (e.g., gates) to monitor progress against requirements conformance, cost, and schedule. Major checkpoints include System Functional Requirements, Preliminary Design Review, and Critical Design Review (additional checkpoints include test, production, and other sustainment milestones). A&D companies have their own product development process that usually incorporates a disciplined checklist.

##### *Issues/Gaps/Misconceptions*

1. Misconception: Design reviews are not necessarily stopgaps for all issues. Preparation is required to assure that all key concerns are addressed concurrently with the completed design rules.
2. Gap: Checklists and heritage knowledge by the review board members do not include Pb-free design considerations.

##### *Conclusions*

Design reviews may lack appropriate oversight of Pb-free impact and risk mitigation to product development.

##### *Recommendations*

1. Exploit a set of Pb-free design rules (Section 3.4.9) as part of the disciplined product development process, and document compliance.

2. Document part finishes, solder materials, fluxes, verification methods and data used to confirm compatibility with assembly processes and life cycle requirements.
3. Document Pb-free part sensitivities to temperature and moisture, and confirm compatibility with assembly/repair processes.
4. Document whisker risk mitigation methods applied for pure tin finishes and Pb-free tin alloys.
5. Document that the design and construction meets the life cycle application, environmental, and operating profiles. Section 7.0, Reliability, identifies particular failure mechanisms pertinent to Pb-free application that require consideration.

### 3.4.7 Quality Assurance ESS and Lot Acceptance Test

#### *Current Baseline Practice*

Acceptance testing has two options: (a) fractional lifetime testing of 100% of product (ESS, “screen” on hardware to be fielded) or (b) full lifetime test on lot-samples (destructive testing). Acceptance testing is performed during the manufacture of fielded hardware to assure that product design specifications are being met. Requirements: Establish the qualification test parameters based upon (a) the computational model, which correlates the accelerated aging test parameters to service life conditions, and (b) the ALT/HALT testing, which bounds the accelerated aging test parameters so that they only activate the service life failure modes.

#### *Issues/Gaps/Misconceptions*

1. Gap: Lacking models, it is unclear what the minimum ESS amount of testing (level and duration) needs to be in order to assure that infant mortal failures are screened and that subsequent service life is maximized.
2. Gap: Methods used to tailor ESS random vibration profiles require accurate models to be effective.

#### *Conclusions*

An effective acceptance test is critical to assure that manufactured products, using Pb-free solder interconnections, consistently meet quality requirements. Applicable test parameters can be developed from validated high fidelity computational models, which correlate acceptance test parameters with service life reliability requirements.

### 3. Design

---

#### *Recommendations*

1. Computational models must be developed which include supporting mechanical and physical properties data, so as to define acceptance testing parameters that are based upon service life requirements. This approach avoids potential reliability and cost penalties that result from under testing or over testing, respectively, because of poorly-defined test variables.
2. Utilize a diverse set of Pb-free electronic assemblies to develop vibration ESS level tailoring to correlate minimum levels needed to find defects in materials and workmanship without substantially reducing service life.
3. Consider adding a section on quality assurance testing in a revision to GEIA-STD-0005-3.

#### **3.4.8 Product Qualification Test**

##### *Current Baseline Practice*

Qualification testing (also known as design verification) is verification of the design in conforming to all requirements. Qualification testing is planned at the requirements stage (see Section 3.2.9) and is typically performed per program-specific or company-specific procedures. Qualification test parameters accelerate the life of the Pb-free interconnections by one or multiple service lifetimes. This is achieved by using the hardware design and manufacturing processes that replicate those for fielded product, including any pre-treatments prior to production or after a design change during production.

Once qualification testing is about to begin, three to five years has often transpired between the development of the initial qualifications requirements defined in the contract. It is likely that several improvements in test methodologies may have been found, and need to be considered since the initial contract inception. In fact, the desired Pb-free solder could have changed from the one envisioned in the first requirements draft. Whatever the reason, it is likely that during the finalization of the qualification test method development, some changes will be needed.

##### *Issues/Gaps/Misconceptions*

1. Gap: There needs to be a way to make adjustments to the qualification requirements, and potentially the contract, based on the most recent Pb-free reliability and failure mode information.
2. Gap: There is the need for a high fidelity computational model which can predict the fatigue of Pb-free interconnections in order to establish acceleration factors required to correlate accelerated test parameters to service life environments.

3. Gap: Solder and PCB material properties (mechanical and physical) are needed to provide input parameters and first-level validation data of such computational models.
4. Misconception: Qualification testing, scoped and budgeted during the contracting phase, should be reassessed since it may no longer capture the new Pb-free assembly failure mode information that has transpired over the three to five years of product development. The qualification tests may not stress newly defined Pb-free failure modes, or may significantly over-test the assembly.

#### *Conclusions*

Computational models are critically needed in order to develop qualification test parameters that are based upon service lifetime requirements, not “lower bounds benchmarks,” thus avoiding either under design or over design of the Pb-free solder interconnections.

#### *Recommendations*

1. Develop a high fidelity, computational modeling capability for predicting fatigue failures of Pb-free solder joints that can readily accommodate varying conditions of temperature cycling, temperature shock, vibration, and mechanical shock. The model must be sufficiently versatile to address past, present, and future Pb-free interconnection designs and materials sets.
2. Establish an extensive mechanical and physical properties test program to provide critical input and first-level validation data for the computational models.
3. Develop provisions for adjusting the qualification test requirements, and possibly the contract, to consider the most recent Pb-free test, modeling, and failure modes data.
4. Structure contracts, schedules, and systems engineering management plans to accommodate a review of the qualification test plan, so that the most current methods can be considered.

#### **3.4.9 Closure**

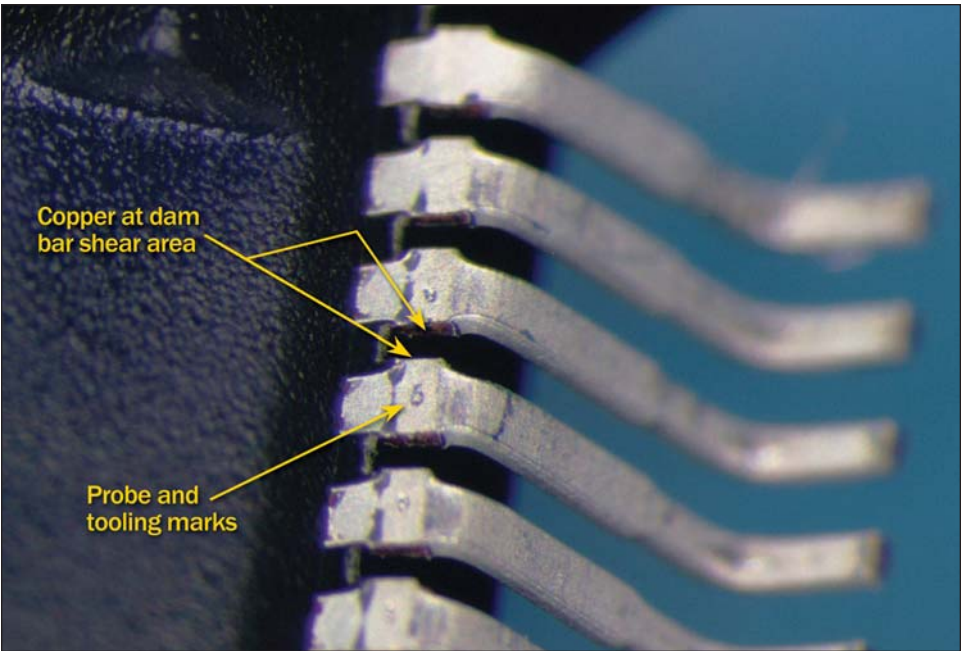
Given the risks identified with Pb-free technology integration, three high level outputs are considered technical imperatives for success in product deployment:

1. Generation of Pb-free design rules.
2. Robust design reviews with appropriate Pb-free checkpoints. Note that a similar discipline is being used in A&D for tin whisker risk.
3. Development of failure models and appropriate test parameters are a technical imperative.

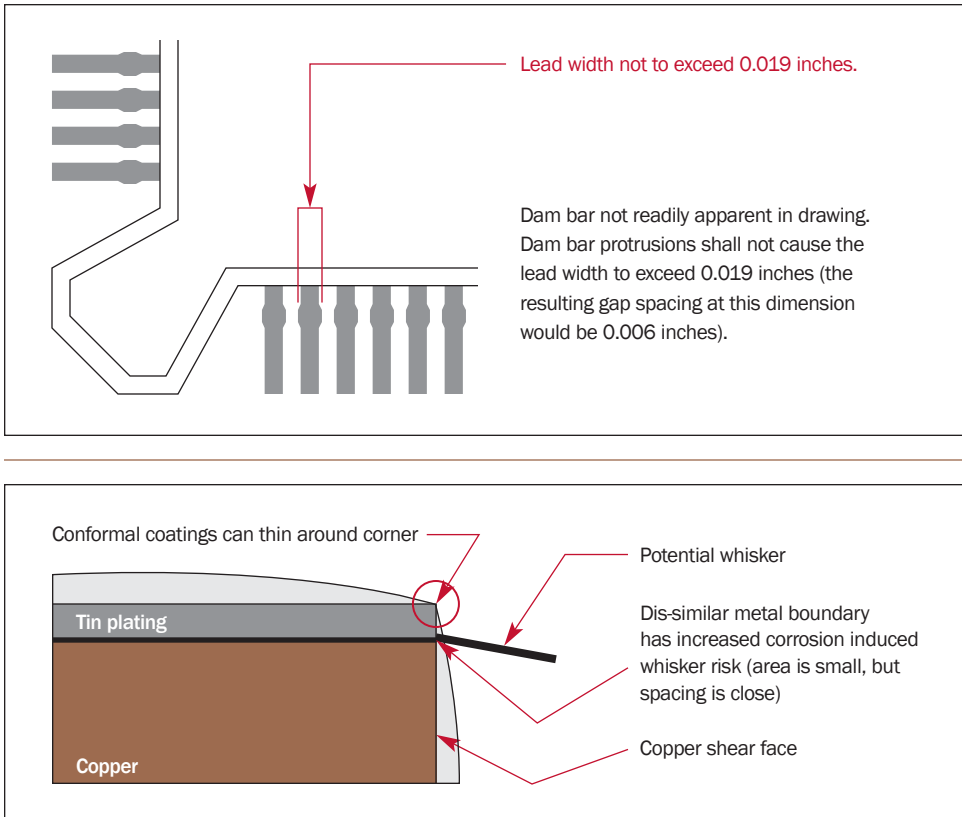
### 3.5 TIN WHISKER RISK ASSESSMENT

#### Current Baseline Practice

The phenomenon and risk mitigations are described in Section 7.0, Reliability, GEIA-STD-0005-2 and GEIA-HB-0005-2. The commercial industry has adopted JESD 201 as its standard for tin whisker acceptance testing. This standard has resulted in major issues for the A&D industry, as it is not recommended for use on high reliability, class 3 products and omits reporting of corrosion induced whiskering. As shown in Figure 3.17, fine pitch microcircuit leads are comprised of many features, such as probe marks and dam bar shear areas, not readily apparent on the procurement drawing. Spray conformal coatings, such as acrylic or polyurethane, can have difficulty covering behind fine pitch leads completely and can fracture due to the tin whisker growth. Some organic coatings can “tent in” a whisker as long as the coating is thick enough. A recently developed ceramic coating applied by vapor deposition, has shown potential in inhibiting growth on a whisker under conditions of high humidity, but the results have not been verified for long term.







**Figure 3.17** The image shows fine pitch microcircuit leads, probe marks and dam bar shear area that not readily apparent on the procurement drawing [20].

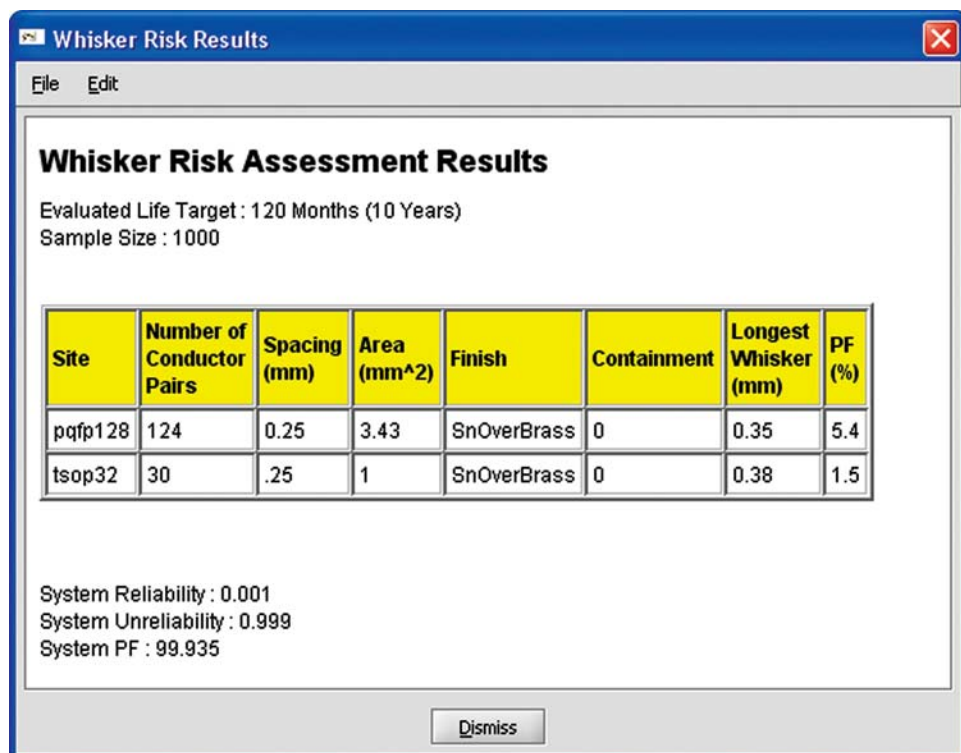
Although not formally accepted as standards, there are two models currently available to assess risk. The CALCE Tin Whisker Risk Calculator [21] presents risk based upon growth factors (length, density) of whiskers. An alternative tool, developed by David Pinsky [22], is an algorithm which is application-specific, considering design factors such as conductor spacing, lead content in plating, deposition process, conformal coating, etc.

### 3. Design

#### Issues/Gaps/Misconceptions

1. Gap: There is still some lack of understanding of the tin whisker phenomenon. Therefore, there is still some lack of understanding as well as appreciation of the assessment tools.
2. Gap: JESD 201 is not adequate as a tin whisker acceptance or risk assessment standard within A&D service conditions. It was originally intended to be a process evaluation tool for data comparison. The cited test conditions are not indicative of actual A&D service environments and, therefore, results are insufficient to assess reliability with respect to potential failures due to tin whiskers. In particular, JESD 201 specifically excludes reporting of corrosion induced whiskers exceeding the maximum allowable limits.
3. Gap: While consumer products have focused on humidity and thermal cycling in the tin whisker testing, A&D equipment is subjected to many diverse environments that can cause compressive loads in the tin such as: corrosive environments, handling, vibration, shock, and probe marks during trouble shooting.
4. Issue: Use of the current baseline practice tools will require application based decisions.
  - The CALCE tool presents risk based upon growth factors (length, density) of whiskers (Figure 3.18).
  - The Pinsky algorithm is application specific in considering design factors, but by itself does not guarantee compliance to GEIA-STD-0005-2 (Figure 3.19).
  - Individual companies also implement specific assessment methodologies, combining the various methods and internal practices to comply with GEIA-STD-0005-2 requirements.

Site ID	Number of Pairs	Conductor Spacing (Gap) mm	Conductor Area mm <sup>2</sup>	Conductor Finish	Coating Containm %
pqfp128	124.0	0.25	3.43	SnOverBrass	0.0
tsop32	30.0	0.25	1.0	SnOverBrass	0.0



CALCE Tin Whisker Risk Assessment Software:

A software package that calculates the probability of tin whisker failure for circuit card assemblies and products. Based on long-term test data.

Figure 3.18 CALCE Risk Mitigation Model. Courtesy of Dr. Michael Osterman, University of Maryland CALCE EPSC [21].

3. Design

Risk Factor					Enter Your Values Here					
Conductor spacing (mils)	<10	10-50	50-100	100-500	>500					
r(1)	5	1	0.25	0.15	0	1				
Pb content (wt%)	<0.2	0.2-1	1.0-2.0	2.0-3.0	>3.0					
r(2)	1	0.2	0.1	0.01	0.0005	1.00				
Process	electroplate		Immersion		Hot dip		Individual factors	values		
r(3)	1		0.3		0.1	0.1	r(13)	1.000	R(density)=	1.166
Tin thickness (micro-inches)	<50	50-250	250-500	500-1000	>1000		r(2)	1.000	R (length)=	0.006
r(4)	0.7	1	0.7	0.3	0.1		r(3)	0.100	R (p)=	0.006
Material directly beneath tin	brass/bronze	copper	ferrous	nickel	other		r(4)	1.000	R(ste)=	1
r(5)	1	0.7	0.5	0.05	0.5	0.06	r(5)	0.060	R(sx)=	0.1
Substrate controlling CTE	ceramic	low expansion alloy	Cu or Al	ferrous	other		r(6)	1.000		
r(6)	1	1	0.2	0.3	0.5		r(6a)	1	R(sx)=	0.006996336
Plating heated after deposition	no		annealed		fused		r(8a)	1.000		
r(7)			0.5		0.2	1	r(9)	0.100		-2.155126354
Conformal coat	none	urethane > 1mil	silicone > 1 mil	polyurethane	epoxy	acrylic	r(10)	0.200	output	6.14
directly on tin surface - r(1a)	1	0.15	0.25	0.10	0.15	0.45	r(11)	0.400		
on adjacent conductors - r(1b)	1	0.05	0.05	0	0.05	0.05	r(12)	0.100		
Use of Mechanical HWDC	testers compressed onto surface		none				K	8.9		
r(9)	1		0.1			0.1				
Where was assembly performed	Clean Room	Special clean area	Typical Factory	Field assembly						
r(10)	1	0.5	0.2	0.1		0.2				
exposed shorting sites with in enclosure	many	some	few	almost none	none					
r(11)	1	0.7	0.4	0.1	0.01	0.4				
Airflow within assembly	Forced air		Dynamic Use		none					
r(12)	1		0.5		0.1	0.1				

Figure 3.19 Pinsky algorithm uses design factors to aid in determining a tin whisker risk level [22].

Conclusions

- 1. A&D equipment is exposed to many diverse environments (long term storage, thermal cycling, vibration, shock, handling, humidity, corrosion, altitude, vehicle and cleaning fluid exposure, etc.) which may result in stresses in the tin finishes or solder, promoting tin whisker growth.
- 2. The use of JESD 201 is in itself a risk because cited test conditions are not indicative of A&D harsh environments, and cannot be extended to provide long term performance.
- 3. Relative risk assessment for tin whiskers has progressed such that the CALCE and Pinsky models are recognized as viable approaches. However, fundamental whisker growth models and additional failure data is lacking.

Recommendations

- 1. Tin whisker risk needs to be incorporated as part of electronics reliability modeling.
- 2. Current tin risk mitigation tools should be integrated into current reliability models to include tin whisker risk in predictions. Note that release of GEIA-HB-0005-4, *Guidelines for Performing Reliability Predictions for Lead Free Assemblies used in Aerospace and High-Performance Electronic Applications*, is imminent and includes a discussion advising that a process be implemented to mitigate tin whisker risk, but is still lacking a model.

3. Begin long term tin whisker testing on actual manufactured assemblies and subject them to simulated A&D environmental conditions of humidity, altitude, vibration, shock, corrosive environments, etc, to evaluate mitigation effectiveness, as well as whisker growth.
4. Encourage fundamental research in tin whisker growth and mitigation effectiveness to improve whisker growth models, so that fundamental whisker growth modeling can be integrated with the long term testing and the reliability modeling.
5. Develop a manufacturing process test coupon for the evaluation of CCA tin whisker growth susceptibility and mitigation effectiveness. If required by the customer, these coupons could be retained for future examination by the equipment manufacturer for many years, much like PCB coupons are retained today.

## 3.6 RELIABILITY ANALYSIS DATA ITEM

### Current Baseline Practice

For A&D systems, it is commonly required that various forms of reliability predictions be performed. These predictions occur during the design phase, as a check that the design is adequate to meet the requirements. The most widely used standard in making reliability predictions for A&D systems is MIL-HDBK-217, although its use is far from universal. Section 16.1 of the handbook includes a model for predicting reliability of PCBs with PTHs; in section 16.2, there is a model for predicting reliability of SMT solder joints. These models are based upon an assumption of exclusive use of eutectic tin lead solder attachment processes and compatible materials. This handbook does not include any models for Pb-free solder attachment processes and compatible materials. The issue of tin whisker induced failures is not dealt with whatsoever.

### Issues/Gaps/Misconceptions

1. Gap: The adequacy of predictions arrived at using MIL-HDBK-217 do not account for Pb-free issues.
2. Issue: A new industry standard, GEIA-STD-0009 has just been released, and may provide an improved, updated approach to reliability prediction.
3. Issue: The LEAP-WG is preparing a document (GEIA-HB-0005-4) that is intended to provide guidance for the performance of reliability assessments of A&D systems, incorporating Pb-free materials and processes. Although detailed models are lacking, it is intended that this document will serve as a basis for the implementation of improved practices.

### 3. Design

---

#### Conclusions

The adequacy of predictions arrived at using MIL-HDBK-217 and other existing documents based upon SnPb data, must be considered suspect.

#### Recommendations

1. When released, the requirements of GEIA-HB-0005-4 should be implemented.
2. It is recommended that the working team continue to be supported to include performing future updates and refinements.

## 3.7 SAFETY AND NON-SAFETY SYSTEMS CERTIFICATION

#### Current Baseline Practice

Avionics products must be qualified and certified for safety for flight application on commercial aircraft. Some Federal Aviation Administration (FAA) circulars regarding Pb-free have been issued and the FAA has participated in the generation of Pb-free risk management industry standards.

#### Issues/Gaps/Misconceptions

There are no issues, gaps or misconceptions to report; however, let it be noted that the first safety certified Pb-free assembly will undergo extensive testing and scrutiny.

#### Conclusions

The requirements for certification do not change for Pb-free.

#### Recommendations

A phased implementation of full Pb-free avionics products should begin with monitored reliability of non-critical systems to gain real product field experience and demonstrate reliability and sustainability.

## **3.8 MANUFACTURING HANDOFF**

### **Production Readiness and Manufacturing Technical Data Package**

#### *Current Baseline Practice*

The transition from design to production is critical to product success. This process is facilitated by involving the manufacturing organization as part of the design team early in the design process. Within this section, production readiness reviews, manufacturing technical data packages, and sustainment technical data packages are discussed.

Most companies conduct production readiness reviews in accordance with their own internal product development system. Most of these systems were generated around the points of MIL-STD-1521 (despite its cancellation in April, 1995). Both manufacturing and sustainment technical data packages, likewise, are generated in accordance with local process. MIL-DTL-31000C may be used as guidance for these particular processes.

#### *Issues/Gaps/Misconceptions*

Production Readiness Reviews, in general, do not include specific flags to address risk and/or challenges of Pb-free implementation. As a result, manufacturing technical data packages could be deficient.

#### *Conclusions*

Production Readiness Reviews and Manufacturing Technical Data Packages, while generally conforming to sufficient industry best practices in terms of content, and schedule of product life cycle, may not necessarily include risks associated with Pb-free technology.

#### *Recommendations*

Implement an awareness/communications campaign to emphasize the need for the following:

1. Pb-free risk assessment and mitigation plans in product development systems at the company level.
2. Pb-free part identification should be supplied by engineering in the Manufacturing Technical Data Packages, for applications where Pb-free finish tracking is necessary.

## 3.9 SUSTAINMENT HANDOFF

### Current Baseline Practice

Sustainment includes support for repair, supply chain for spares, and end-of-life. The current baseline practice for repair of CCAs, and other assemblies, is based on the assumption that SnPb is used for CCA assembly, and that SnPb-compatible coatings are used for printed wiring board bond-pad and finish coatings on the terminations of the piece parts. This assumption is so widespread that not all program requirements include the use of SnPb, even though it is assumed. Very few A&D customer requirements have been updated to include Pb-free electronics.

### Issues/Gaps/Misconceptions

1. Gap: Documentation will require assessment for Pb-free impacts to assure incorporation of sufficient information which allows for successful spares procurement and repair action
2. Gap: Repairability verification requires assessment of reliability after repair, with consideration for degradation mechanisms that affect Pb-free assemblies in the field.

### Conclusion

Documentation will require revisions to address Pb-free impacts.

### Recommendations

1. Identify part finishes and solder alloys used on assemblies per J-STD-609, and specify repair solder alloys and processes that assure sufficient reliability.
2. Provide inputs to repair procedures and manuals to assure reliability of repaired equipment.
3. Provide effective qualification requirements for spares procurement, and change re-qualification procedures which take into account Pb-free materials properties and reliability requirements.



“The brain is a wonderful organ.

It starts working the moment you get up in the morning  
and does not stop until you get into the office.”

—*Robert Frost (1874-1963)*



# 4. Manufacturing

## 4.1 INTRODUCTION

The advent of Pb-free solders and materials into the manufacturing stream has posed new challenges for OEMs and CMs alike. New Pb-free solder alloys are continually being developed, while investigations into new solder-less technologies are concurrently being pursued as alternates to the conventional means of attachment. Pb-free electronics manufacturing requires tighter process controls, with more rigorous attention to the detailed requirements for each process flow step than for SnPb systems. Implementation of process control windows and variables is essential for assembly of Pb-free electronics. Understanding the importance and the method of good solder joint formation is critical to solder joint integrity. The metallurgical aspects of solder joint formation will be discussed as a prelude to the manufacturing processes because of the critical nature of how solder joint formation sets a foundational basis for establishing process parameters. Design for manufacturing is also particularly vital as an implementation tool in the understanding of the factors related to high yield, low cost assemblies. With the addition of the new Pb-free material sets, which includes solders, finishes, and substrates, defect detection becomes more difficult because the failure mechanisms are either not fully defined, or considerably different than SnPb. Despite the lack of Pb-free “drop-in” practices, manufacturing a Pb-free assembly is possible with improved process controls, targeted design modifications, and equipment selections. The following flow chart depicts the baseline practices of each step in the manufacturing flow. The blocks in the flow chart are color coded to depict areas that are impacted (and to what degree) by Pb-free processing.

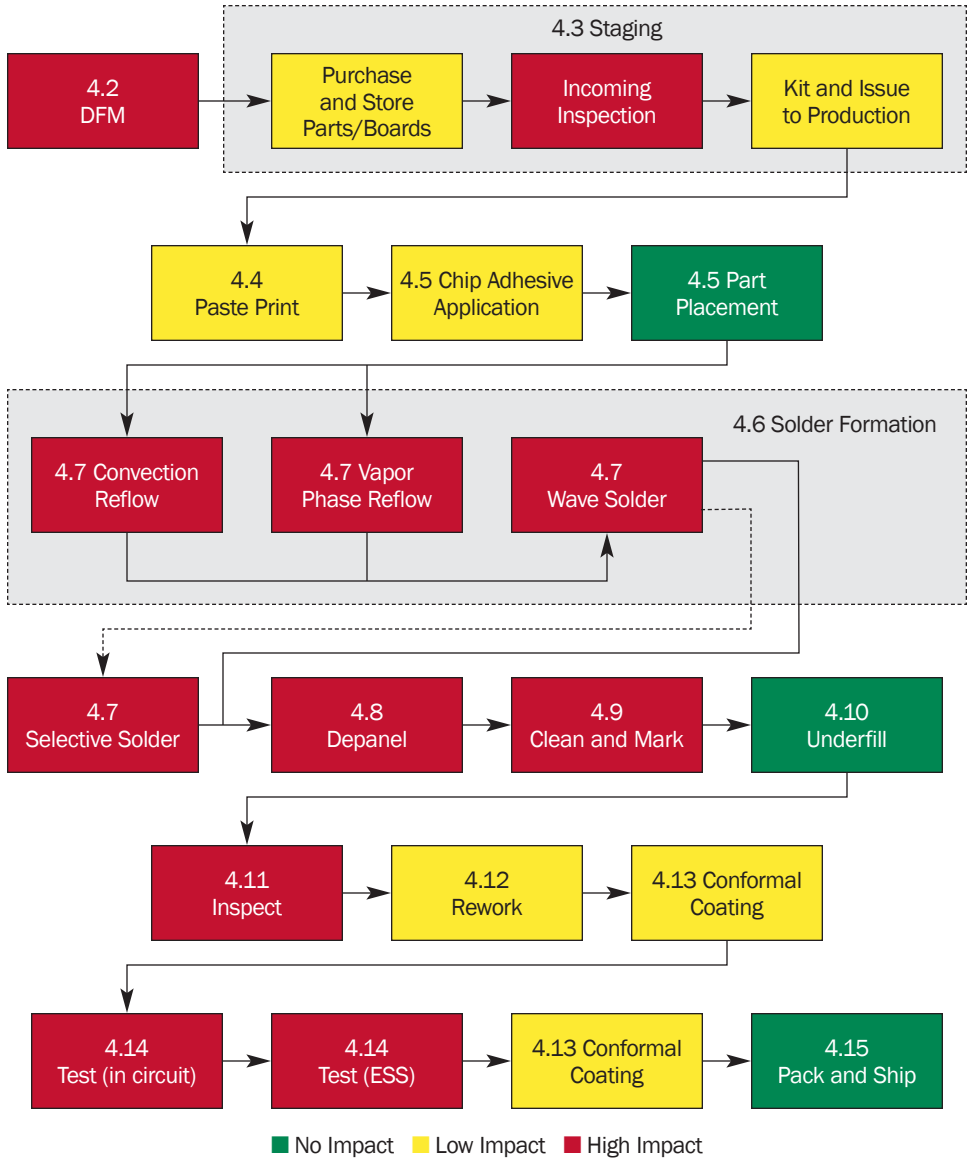


Figure 4.1 Manufacturing Flow. The blocks in the flow chart are color coded to depict areas that are impacted (and to what degree) by Pb-free processing.

### 4.2 DESIGN FOR MANUFACTURING

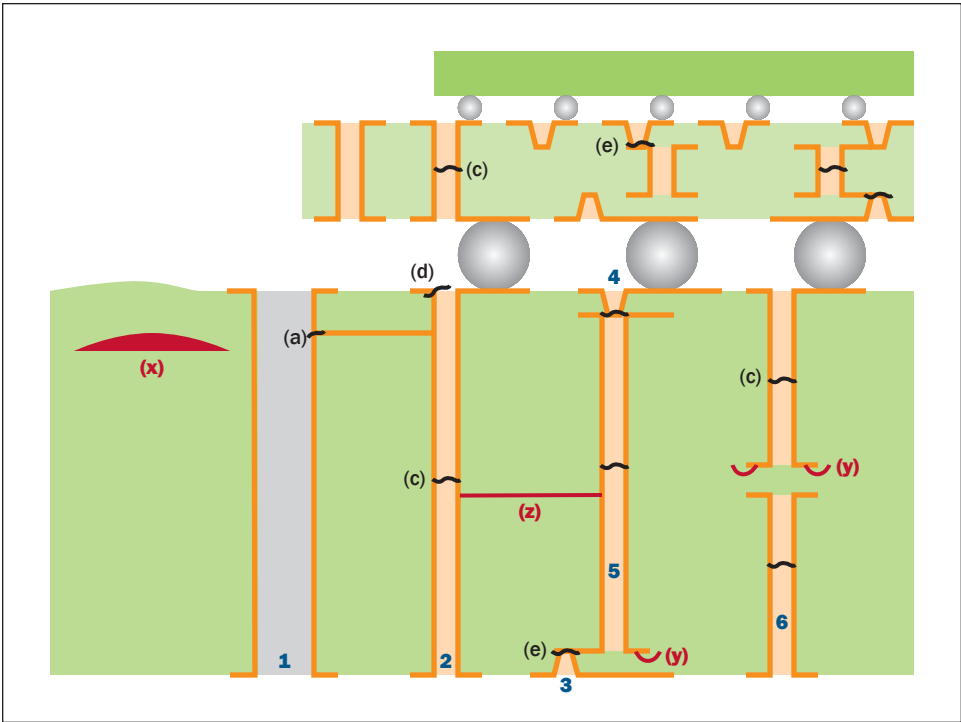
#### **Current Baseline Practice**

The following sections will provide details for the baseline practices and design rules for Pb-free manufacturability including PCB issues, component issues, solderability, assembly layout, work area strategies, training, process qualification protocols, and first article inspection.

#### **Issues/Gaps/Misconceptions**

##### *Printed Circuit Boards*

The implementation of Pb-free solder processes will have several minor impacts on how PCBs are handled within the manufacturing process. The impact of Pb-free processing on printed circuit board laminates are covered in the Design segment of this report (Design Section 3.4.6). It is also anticipated that the IPC-6012 specification will contain Pb-free electronics-driven laminate requirements [1], and the board fabricator will see a greater burden of proof in “certifying the product” for Pb-free. However, little change will occur in the printed circuit board fabrication processes. Pb-free solder processes have a greater reliance on the solderability of a PCB and the solderability requirements of the IPC J-STD-003 should be followed [2]. The manufacturing process window is increased by the use of improved CCA storage and handling protocols. Some Pb-free qualified laminates may require baking depending on the laminate material characteristics and the use of enhanced PCB packaging techniques, as detailed in the IPC-1601 Board Storage and Handling Standard [3]. The plated through hole has changed considerably during 50 years of electronic packaging; however, despite its many forms, it remains the most common interconnection in first and second level electronic packaging and one of the most worrisome in terms of reliability. The transition from the original solder filled holes to BGA wiring vias, sub-composite buried vias, and today’s micro-vias has resulted in many new failure mechanisms, not only in the copper interconnections, but also in the surrounding laminate – especially with the requirements for the higher temperature Pb free reflows (Figure 4.2).



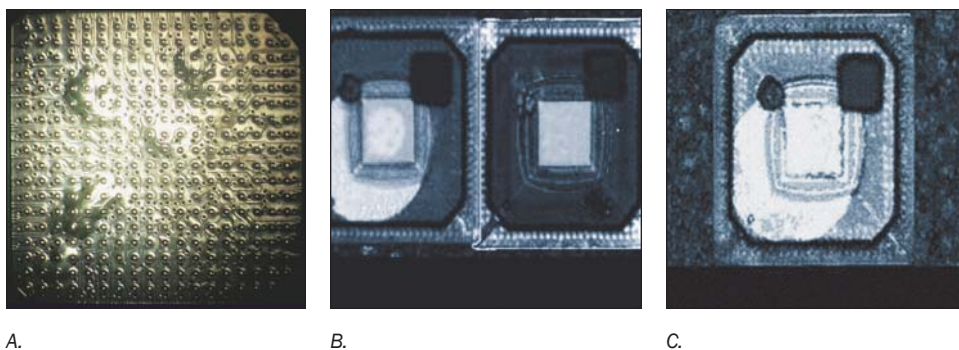
**Figure 4.2** The “PTH” family and related failure mechanisms for today’s boards and chip carriers. All are being made more severe by the higher temperatures needed for Pb-free electronics manufacturing. Via 1 is a standard size via and 2-5 are micro vias including blind and buried. Letters a-z indicate assorted defect failure modes, including barrel cracking, eyebrow cracking, and laminate cracking.

- CCAs: General handling procedures of CCAs will require improved “due diligence” as the CCAs and Pb-free solder joints are more prone to bending damage with respect to typical assembly handling. Increased care should be exercised for tasks such as CCA tote insertion/removal and other actions that induce bending of the assembled or partially assembled CCAs.
- Components: New component material sets are emerging as the industry transitions to Pb-free. It is crucial to understand the materials in the components and any sensitivities or compatibility issues that may be encountered during the assembly process.

## 4. Manufacturing

---

Manufacturing processes for Pb-free assembly require higher temperatures and place more risk on components that may have temperature sensitivity (Figure 4.3). These components have been labeled TSC (temperature sensitive components) and the IPC has developed specifications to describe the precautions for their use (J-STD-075) [4]. The other issue to be aware of is that many components have only been tested and qualified for the SnPb solder process, and many have a maximum temperature rating of 225-230 °C. Additional testing and qualification will be required to rate these components to a higher Pb-free rating of 250-260 °C. The moisture sensitivity levels (MSLs) must also be revised to ensure the components won't be damaged during the Pb-free soldering process. The MSL rating goes up to a higher level per J-STD-020 classification and likewise, must be handled more stringently per J-STD-033 [5, 6] for Pb-free assembly.



**Figure 4.3** Delamination (“popcorning”) of various components due to inadequate bake before reflow – more prevalent in the higher-temperature Pb-free processing than in the traditional SnPb processing. Photo A is courtesy of Steve Gregory, OAI Electronics. Images B and C are courtesy of Lockheed Martin.

### Component Alteration Processes

The implementation of Pb-free solder processes has significantly impacted the traditional component alteration processes of “hot solder dipping” and BGA solderball replacement. Typical Pb-free solder alloys melt at 217 °C, which is an increase of 34 °C from conventional SnPb solder alloys. The increased temperature can cause degradation of components subjected to alteration if adequate process controls/parameters are not implemented. Component alteration processes need to have the solder alloy requirements, thermal management, bath contamination control, and specified removal/attachment parameters defined for Pb-free alloys. The component alteration procedures should be subjected to a qualification assessment that includes both material selection and procedure review. Analytical techniques such as ultrasonic inspection and hermeticity testing should be conducted to assess the component integrity as part of the component alteration process qualification.

### Assembly Layout

**Color coding of product.** It is an industry best practice to have a master manufacturing facility layout strategy for either the coexistence or the segregation of SnPb and Pb-free soldering processes. Cross contamination of SnPb and Pb-free soldering process flows should be avoided due to potential product reliability issues. The available facility space will play a role in the process layout strategy. The optimum layout strategy is to have physically separate, segregated assembly flows and tools. Utilizing separate, segregated assemblies flows/tools is the simplest strategy to avoid process cross contamination. An alternative layout strategy is to utilize color designations, color label schemes, and separate solder process tool “kits,” so that the SnPb and Pb-free assembly processes coexist within the same process flow. A variety of commercially available color designation materials (green ESD mats, colored soldering iron handles, etc.) or internal label/markings strategies (Figure 4.4) can be used. The utilization of color designations/labels for solder materials (e.g., solder paste tubes, solder wire, solder wick) is recommended. Finally, color coding of CCAs for visual identification/recognition is an industry best practice. The designation of a specific soldermask color (e.g., Pb-free CCAs use blue soldermask, SnPb CCAs use green soldermask) allows for immediate CCA process identification for process personnel.



**Figure 4.4** Assembly equipment utilizing color marking, designating them as part of a Pb-free solder process only CCA flow. Photos A and B are courtesy of Rockwell Collins; image C is courtesy of Stanley Supply Services.

### Marking Strategy

The high temperatures of wave and/or reflow soldering of Pb-free product will require that the bar code marking of the individual CCAs be done using laser marking or equivalent high temperature bar code labels. The high temperature label is usually made of a polyimide material with a high temperature adhesive backing. The development and implementation of laser marking is another heat-resistant method to permanently and directly apply a bar code label onto the CCA. Marking the solder alloy on the assembly is recommended if the technical data package does not state the solder alloy material. IPC standard IPC-609 defines the “E” code designations for different solder alloys.

## 4. Manufacturing

---

### *Manufacturing Personnel Training*

A common misconception is that there is no operator training required for switching from SnPb to Pb-free manufacturing technology. Operator training is needed to define and teach the differences of Pb-free processing. Training time should be allocated to transition from SnPb to Pb-free electronic assembly, so that operators trained in the soldering and inspection of SnPb based CCAs can adjust to the issues that accompany the switch to Pb-free. The differences between SnPb and Pb-free electronics hand soldering process techniques can be addressed with four to eight hours of training for operators with only SnPb manufacturing experience.

Areas where operator training will result in better and more efficient Pb-free manufacturing:

- Keeping SnPb and Pb-free materials, fixtures, fluxes, soldering tips and equipment separate from Pb-free.
- The inspection of solder joints for Pb-free alloys should follow the IPC A-610D.
- Training in manual soldering of Pb-free alloys and fluxes to minimize icicle, open and short defects.
- Instruction on finished CCA handling for the minimization of stress on component solder joints when placing process or finished CCAs into totes, cabinets, or test fixtures.

Inspection to IPC A-610D Pb-free product acceptance is sometimes erroneously assumed to be all that is necessary to qualify a facility to manufacture Pb-free electronics. This is not necessarily sufficient. A facility should develop a Pb-free control plan in accordance with GEIA-STD-00005-1, as objective evidence of Pb-free solder process readiness [7]. Self-proclamation of that readiness is adequate for most well-established OEMs to declare and thereby satisfy the customer. Another common misconception is that IPC or other third-party Pb-free electronics manufacturing certifications, while potentially useful, are sometimes erroneously assumed to be required to qualify a facility to manufacture Pb-free electronics. Engineering awareness training will also be required.

- Process qualification. All processes will have to be evaluated and revised to accommodate new Pb-free materials and process parameters. The following table describes some of the critical parameters that will need to be addressed. The methodologies for these process qualifications do not change, but the process variables and tolerance controls may significantly change.



Process Qualification	Attributes for Pb-Free Processes				
Solder Paste	Compatibility	Tooling Cleanup	Clean Ability	Printability	Reflow
Flux	Compatibility	Tooling Cleanup	Clean Ability	Activation Temperature	Residue Acceptability
Cleaning Chemistry	Compatibility	Tooling Cleanup	Performance	Flux Loading	Residue Acceptability
Chip Adhesives	Compatibility	Tooling Cleanup	Clean Ability	Dispensability	Stencil Capability
Conformal Coatings	Compatibility	Tooling Cleanup	Reworkability	Automated Processes	Coverage Capability

**Table 4.1 Process Qualification Table**

- Assembly for first article inspection. The first article inspection for each new product that is transitioned to Pb-free is critical. The product needs to be assessed for workmanship and compliance to the engineering technical data package. All processing and workmanship issues need to be resolved before continuing to process products on the Pb-free assembly line. Equipment and/or process parameters may need to be adjusted to improve yield. Due to the tighter process control windows and added complexity in assessing solder joints, Pb-free assembly processing must be closely scrutinized and controlled.

## Conclusions

DFM is critical for high yield Pb-free manufacturing. All aspects of the design must consider the use of Pb-free processes including PCB and component issues, training, process qualifications, and first article inspections. The transition of a printed wiring assembly from a SnPb soldering process to a Pb-free soldering process requires a mandatory DFM assessment.

## Recommendations

Implementation of stringent DFM rules and adherence to known design rules (Section 3.0, Design), is critical for Pb-free manufacturing of high reliability electronics. Storage and handling practices will have to be evaluated and enforced. Component TSC and MSL ratings for Pb-free must be followed according to the IPC documents. Altering components requires a process qualification, area and materials segregation, along with color coding to prevent cross contamination. Additional operator and engineering training must be conducted with the necessary time to complete the training. First article inspection of new products transitioning to Pb-free is required, and should be scrutinized carefully to ensure quality. The transition of a printed wiring assembly from a SnPb soldering process to a Pb-free soldering process requires a mandatory DFM assessment.

## 4. Manufacturing

---

### 4.3 STAGING

#### Current Baseline Practice

Staging consists of purchasing, storing parts/boards, incoming inspection, parts screening, and issuing the parts/boards to the production area. Processes are in place for purchasing, storing, and kit issues, but parts screening may need to be adopted if there are restrictions on the type of component lead finishes allowed on a product.

#### Issues/Gaps/Misconceptions

Additional understanding of solderability shelf life requirements for PCB surface finishes and component lead finishes may require the manufacturing floor to store and handle parts/boards differently. SnPb PCBs and SnPb components essentially had indefinite solderability shelf life; however, the Pb-free parts/boards will not. IPC specifications describe solderability testing of parts/boards and must be used to evaluate a particular surface/component finish (Section 6.2.3, *Solder Testing*). This will necessitate shelf life requirements to be invoked and tracking the results of the retesting to be employed. Likewise, the kitting of parts/boards to the manufacturing floor will have to be an integral part of this process.

Component level screening for surface finishes of leads is performed using XRF (x-ray fluorescence) or SEM/EDS (scanning electron microscope/energy dispersive spectroscopy). XRF equipment has been improving, driven by the need for increased analytical sensitivity to meet the Pb-free screening requirements. Bench top type XRF systems are more accurate and reliable than hand held type systems. The typical use of XRF has been to prove that parts/assemblies can be classified as Pb-free, and therefore comply with the RoHS initiative. Some users have product requirements that restrict certain component lead finishes and are using XRF to screen for these prohibited materials (e.g., pure tin electroplate). Current equipment requires detailed calibration using known standards because XRF can provide false readings, both positive and negative, due to the scanning depth of the x-ray used in the process. Screening for pure tin and other unknown finishes may not be accurately detected using this method. SEM/EDS is more accurate; however, the equipment is complex, requires a skilled operator, and has a higher cost. More importantly, XRF is a non-destructive method, while in most cases SEM/EDS requires destructive sample preparation.

#### Conclusions

Changes to the purchase, storage, and screening of parts may need to be improved with the transition to Pb-free assembly. Additional tracking and solderability testing will be required to ensure high yields and uninterrupted production flow. Parts screening may be a requirement on future production assembly for either controlling a product that is to be Pb-free or keeping restricted Pb-free finishes from getting into the product. The concern is unintended intrusions of parts/boards materials from the products being built.

### Recommendations

Tighter controls should be utilized to track and keep parts/boards acceptable and producible. Additional shelf life controls may be required with retest to ensure good solderability during the assembly process.

XRF and EDS must be used to establish a parts screening process. EDS can be used as a barometer to calibrate the XRF equipment. When both XRF and EDS are available, a coarse screening with XRF followed by a finer screening with EDS is recommended.

## 4.4 SOLDER PASTE DEPOSITION

### Current Baseline Practice

Current practices/processes are acceptable for Pb-free. No major changes are required for the solder paste deposition due to the implementation of Pb-free soldering. The solder paste supplier should include process controls, handling, storage and equipment parameters for the specific solder paste product, and should be followed. No changes in stencil material, design and aperture methodology are required.

### Issues/Gaps/Misconceptions

Cross contamination issues (solder paste handling, stencil print wiping, and stencil cleaning) should be addressed as part of a CCA process flow strategy.

### Conclusions

No major changes are required for the solder paste deposition due to the implementation of Pb-free soldering.

### Recommendations

Cross contamination issues (solder paste handling, stencil print wiping, and stencil cleaning) should be addressed as part of a CCA process flow strategy.

## 4.5 COMPONENT PLACEMENT

### Current Baseline Practice

Component placement processes and equipment are mature and established for automated circuit card assembly. No major changes are required for the component placement due to the implementation of Pb-free soldering.

## 4. Manufacturing

---

### Issues/Gaps/Misconceptions

Current industry component placement equipment is capable of accommodating Pb-free materials and CCAs. Minor changes in the lighting levels of the vision recognition system may be necessary depending upon the component surface finish selection. Process controls and process parameter changes may be required for passive component adhesive deposition. The adhesive supplier should include process controls, handling, storage and equipment parameters for the specific adhesive product; these should be followed. Tolerances for placement accuracy need to be tighter to compensate for less self-alignment with Pb-free soldering processes.

### Conclusions

No major changes are required for the component placement due to the implementation of Pb-free soldering.

### Recommendations

Minor changes to the lighting levels of the vision recognition system may be necessary depending upon the component surface finish selection. The chip adhesive supplier includes process controls, handling, storage and equipment parameters for the specific chip adhesive product; these should be followed. Accuracy tolerances must be re-evaluated on placement equipment and adjusted to ensure high yields. For example, surface mount resistors/capacitors components will not “self align” as well with Pb-free solders as with SnPb because of the lower wetting forces of Pb-free solders, requiring extra care in placement.

## 4.6 SOLDER METALLURGY - SOLDER JOINT FORMATION

### Current Baseline Practice

The first phase of the transition to Pb-free solder alloys was based around the tin (Sn) 3.5-3.9% silver (Ag) 0.7-0.9% copper (Cu) (SAC) near eutectic alloys. This was driven initially on various industry consortia projects, such as the National Center for Manufacturing Science (NCMS) alloy down-selection study, and later strengthened by the original iNEMI Pb-free reliability study. Because of concerns about the cost of silver and in the hopes of avoiding a patent held by Iowa State University, the Japanese Electronics Industry Association (JEITA) followed by the IPC, recommended use of the hypoeutectic alloy commonly known as SAC305 (Sn3.0Ag0.5Cu). However, many companies, particularly in Europe, chose to stay with the higher silver SAC405 because of the advantages that a eutectic alloy offers, particularly a lower incidence of shrinkage cavities and a lower melting temperature and pasty range.

The mainstream SAC305 and SAC405 compositions are used currently as solder paste and wave alloys as well as alloys for ball grid array solder balls. The poor mechanical shock performance of SAC305 and SAC405 alloys has driven the handheld (consumer) product segment to consider the development of low Ag or low Cu ball alloys to improve the mechanical strength of BGA and CSP solder joints, especially under dynamic loading conditions. These alloys often have some additional elements for micro-alloying: antimony (Sb), nickel (Ni), bismuth (Bi), phosphorus (P), germanium (Ge), cobalt (Co), indium (In), and chromium (Cr), with several already being used commercially.

Not all products manufactured today utilize Pb-free solders. Those industries and OEMs that qualify for exemptions specified in the RoHS directive are still assembling many of their products using SnPb solder pastes. The challenge for these OEMs has been a shrinking supply of SnPb balled BGAs. In some cases, the use of Pb-free balled BGAs is the only available option. The only recourse is to use the Pb-free BGA in a SnPb soldering process. Therefore, pure Pb-free and mixed metallurgy Pb-free components/SnPb solder assemblies will be discussed in this section. Table 4.2 shows commonly used Pb-free solder alloys.

Solder Alloys	Manufacturing		
	Reflow	Wave	Rework
Eutectic SnPb			
SAC305	> Temperature	Copper Dissolution	Copper Dissolution
SAC387	> Temperature	Copper Dissolution	Copper Dissolution
SAC405	> Temperature	Copper Dissolution	Copper Dissolution
SACBi	> Temperature	Copper Dissolution	
SAC Sb			
SnCu	>> Temperature	Copper Dissolution	Copper Dissolution
SnCuNiGe	> Temperature		
SnCuNiBi	> Temperature		
SnBi			
SnAg			

■ No Impact   ■ Low Impact   ■ High Impact   ■ Unknown

Table 4.2 Pb-Free Solder Alloys Applicable Processes

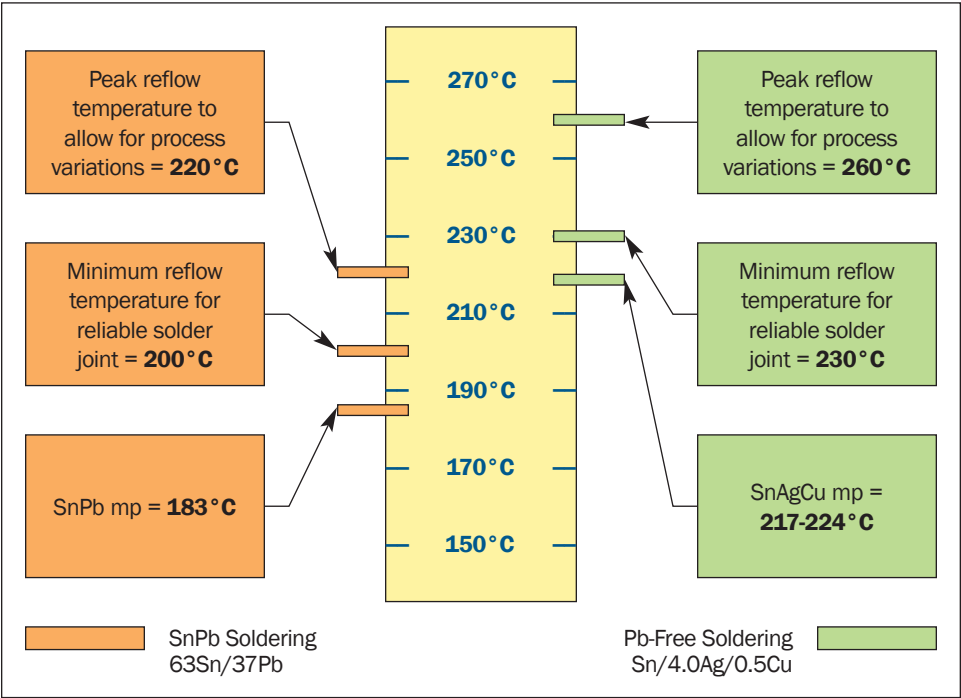
## 4. Manufacturing

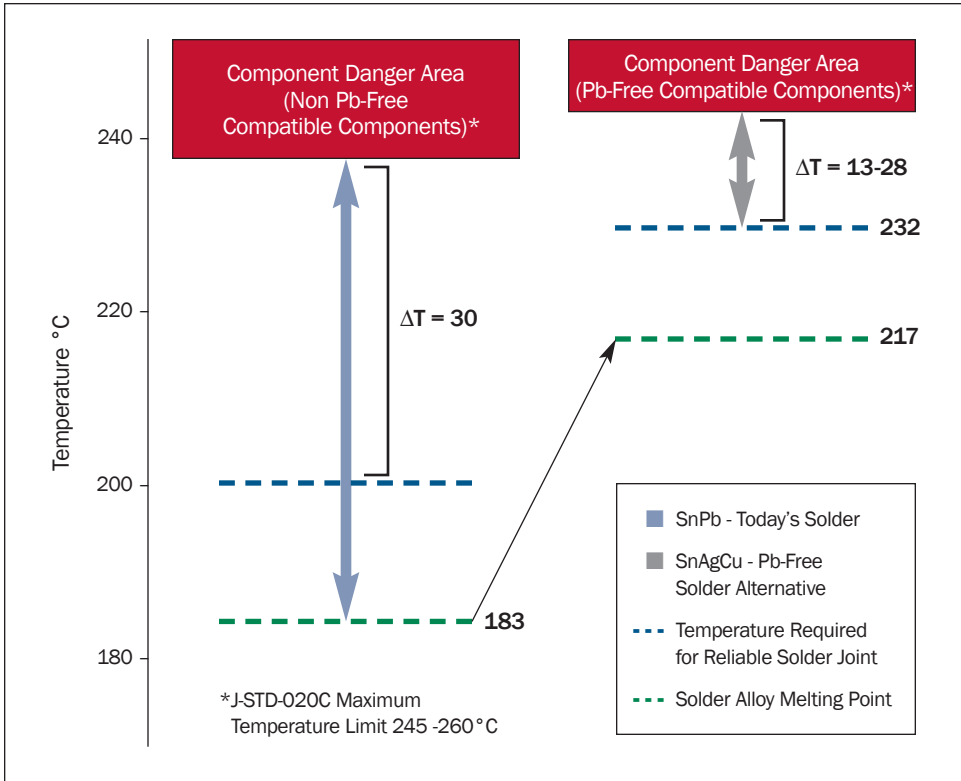
### Issues/Gaps/Misconceptions

The relationships between the Pb-free solder joint microstructure and reliability in different environments are not fully understood.

#### Pure Pb-Free

The mainstream Pb-free SnAgCu alloys have higher melting temperatures than that of the tin/lead alloys (Figure 4.5). The onset melting temperature of SAC alloys is typically 217 °C, which is 34 °C higher than SnPb melting temperatures. When assembling Pb-free components using Pb-free solder, the minimum solder joint temperature on any component on the board should be no less than 230-232 °C to provide a proper wetting [1]. The maximum temperature should not exceed 245-260 °C [2] to assure package and PCB survival. Therefore, the operating window for Pb-free is significantly reduced.





**Figure 4.5** The diagrams show a significant reduction in the Pb-free process window compared to SnPb assembly; this is caused by the difference in melting temperatures and component survival ability. Courtesy of Celestica.

#### Mixed Solder Process

When Pb-free BGA components need to be incorporated into SnPb assemblies, two main scenarios can be considered:

1. The use of a hybrid SnPb reflow process, adjusting the conventional parameters.
2. Design for a reliable mixed assembly when given the optimized manufacturing process parameters.

## 4. Manufacturing

Previous reliability studies on backwards compatibility conducted using SAC305 and SAC405 BGAs soldered using tin/lead paste have demonstrated that by soldering at peak temperatures in excess of 217°C, SnPb solder paste and SAC BGA balls mix completely to form a homogenous microstructure with adequate reliability performance for many electronic applications; however, your specific product must be tested to ensure reliability over the life of the product [3, 4, 5]. The “hot” SnPb reflow should comply with maximum package temperature requirements of the IPC/JEDEC J-STD-020 specification to prevent overheating other components qualified to the tin lead soldering process only. This demanding assembly process involves soldering temperatures higher than conventional SnPb but lower than a full SAC process:

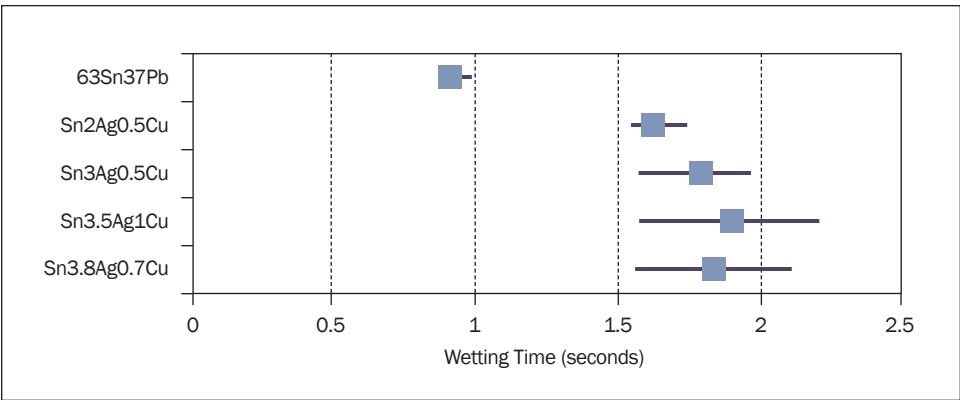
- Temperature minimum at solder joint  $\geq 220^{\circ}\text{C}$
- Temperature maximum package body  $\leq 233^{\circ}\text{C}$

### Wetting Discussion

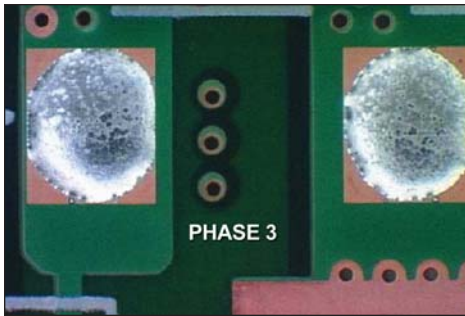
SAC solder pastes have decreased wetting and higher contact angle compared to SnPb as a result of a higher surface tension, lower wetting force and higher wetting time [8]. Low Ag alloys have even poorer wetting than near eutectic SAC305 and SAC405, and as a consequence, the operating process window for Pb-free solder is significantly reduced.

To compensate for the inferior wetting characteristics of Pb-free, it is recommended to:

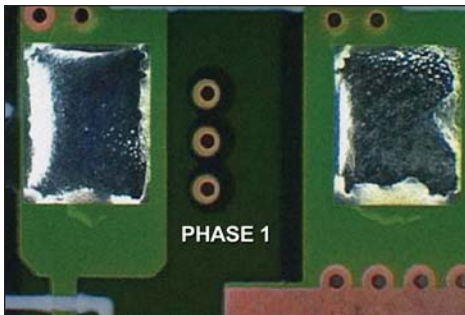
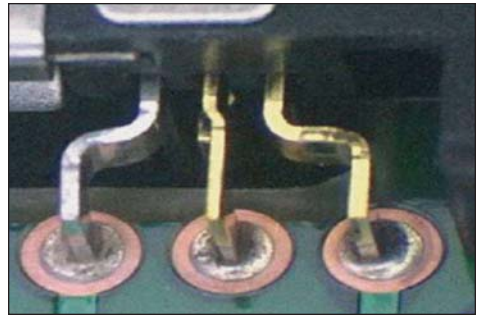
1. Consider sufficient time above melting temperature.
2. Use a new generation of solder pastes with improved fluxes.
3. Perform solder paste qualification to choose the best suited for the specific design and application.



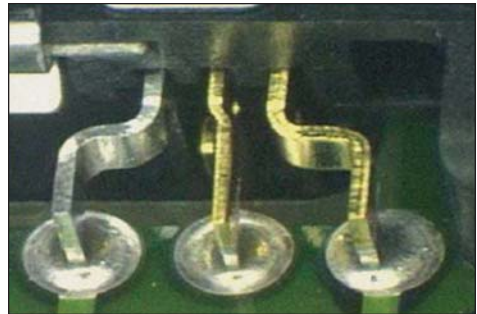




SAC305



SnPb



*Figure 4.6 Solder joint appearance, surface tension and wetting time showing the difference in wetting between SAC305 and SnPb soldering. Photos courtesy of Celestica Inc.; chart from IPC J-STD-033 [6].*

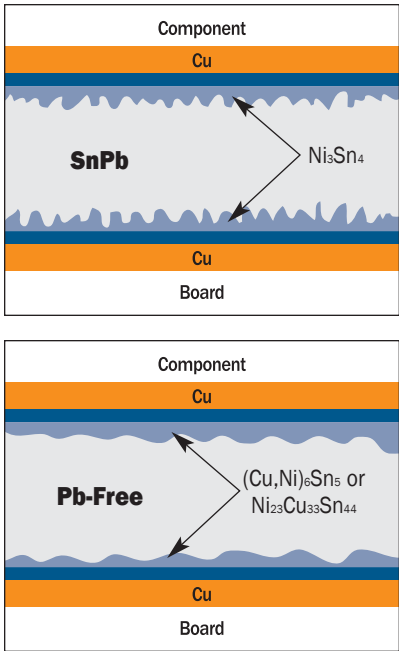
#### Microstructure of Pure Pb-Free

Pb-free solder joint microstructures are quite different from SnPb (Figure 4.6) in the following regard:

- Bulk solder
  - instead of two ductile solid solutions ( $\beta$ Sn) and (Pb) in SnPb, SnAgCu alloy consists of  $\beta$ Sn phase with hard and brittle intermetallic particles
  - instead of smaller, multiple Sn grains, there are several large Sn grains
- Intermetallic reaction layers: different intermetallic types between SnPb and Pb-free
- Intermetallic thickness: intermetallic layer is thicker in Pb-free after assembly and rework

## 4. Manufacturing

Unlike SnPb, which solidifies at a constant temperature, several degrees below melting point, Pb-free joints require significant undercooling. Near eutectic solders like SAC305, SAC387, and SAC405 start to solidify 20 to 40 °C below 217 °C depending on the cooling rate. The crystallization occurs step by step with several changes in which phases are formed as the solder cools. The sequence and phase precipitation depends on solder joint composition and cooling rate. In SAC405, the solder cools slowly, subsequently causing the primary Ag<sub>3</sub>Sn crystals to appear first (Figure 4.7), followed by the pseudo-eutectic Ag<sub>3</sub>Sn + Cu<sub>6</sub>Sn<sub>5</sub> + Sn [9], and the formation of large Sn dendrites. Cooling rates higher than 1.3-1.5 °C/s may prevent primary intermetallic crystals from nucleation. Under those rapid cooling conditions, the Sn phase will appear first followed by Ag<sub>3</sub>Sn + Cu<sub>6</sub>Sn<sub>5</sub> + Sn eutectic [9]. This type of solidification is typical for SAC305 with lower Ag content even if it solidifies under slow cooling conditions. If significant copper dissolves into SAC solder during reflow, the first phase to form is Cu<sub>6</sub>Sn<sub>5</sub>, followed by formation of a combination of Ag<sub>3</sub>Sn and Cu<sub>6</sub>Sn<sub>5</sub>, followed by the formation of the pseudo-eutectic Ag<sub>3</sub>Sn + Cu<sub>6</sub>Sn<sub>5</sub> + Sn, with the formation of large Sn dendrites. This phenomenon will drive tighter control of process temperatures and CCA cooling rates to prevent solder defects.



Me<sub>3</sub>Sn<sub>4</sub>, where Me = Ni and Cu

- On ENIG boards with
  - SnPb solder
  - Pb-free solder - SnPb ball (Cu < 0.2)

Me<sub>6</sub>Sn<sub>5</sub>, where Me = Ni and Cu

- On ENIG boards with
  - Pb-free solder - Pb-free ball (Cu > 0.5)
- On Imm Ag and OSP boards with both SnPb solder and Pb-free solder

Me<sub>3</sub>Sn<sub>4</sub> and Me<sub>6</sub>Sn<sub>5</sub>, where Me = Ni and Cu

- On ENIG boards with
  - SnPb solder - Pb-free ball (0.2% < Cu < 0.5%)



Figure 4.7 Pb-free solder joint microstructure. Photos A and C are courtesy of Celestica Inc.; image B is courtesy of Unovis.

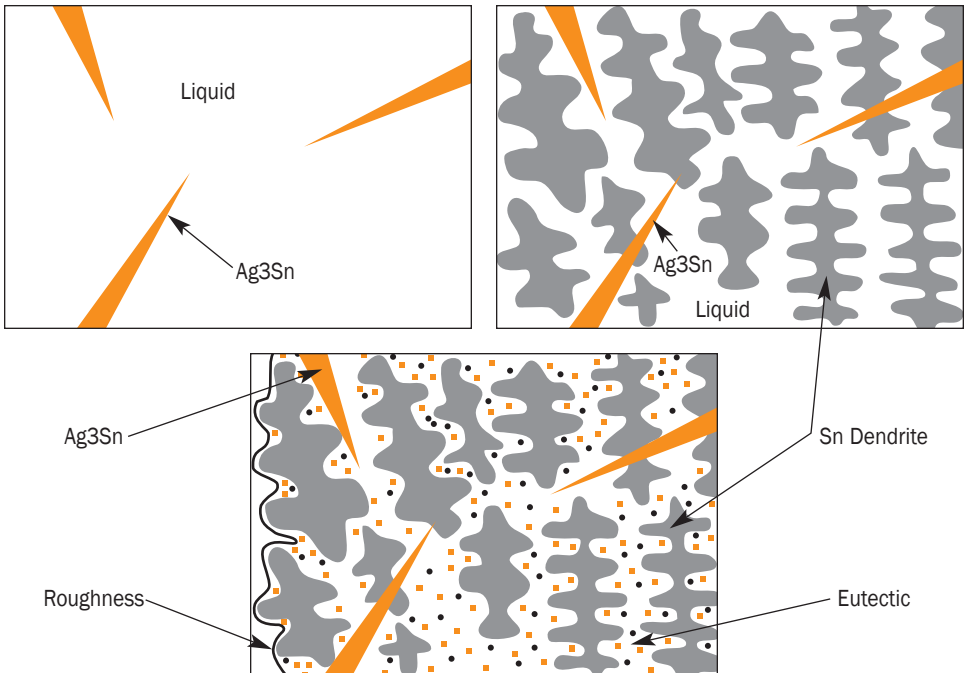
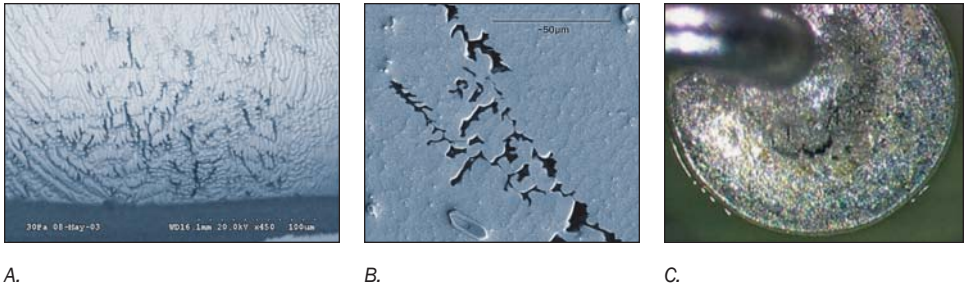


Figure 4.8 Schematic diagrams of the microstructure formation in Pb-free paste; Pb-free solder balls under reflow [7].

## 4. Manufacturing

### Shrinkage Voids

The shrinkage voids form in the last portions of eutectic liquid that are entrapped between the Sn dendrites. The voids usually inherit the inter-dendritic shape (Figure 4.9) [9] and often have dendrite arms visible inside the voids.



**Figure 4.9** Surface roughness and shrinkage voids. Photos A and B are courtesy of Celestica; image C is courtesy of Rockwell Collins.

Pb-free solder joint reliability depends on microstructure and phase compositions. Industry testing has demonstrated that shrinkage voids do not result in a degradation of solder joint integrity.

### Mixed Metallurgy for BGA Solder Processes

When SnPb solder melts at 183 °C during reflow, the SnAgCu solder ball will begin to dissolve in the molten solder (Figure 4.10: a, b) [3]. The dissolution continues until the liquid attains a saturation composition. The saturation level increases with the rising temperature; consequently, the higher the temperature, the larger the portion of the SAC solder ball that is consumed by the molten SnPb solder. For a certain ratio of SAC solder ball and SnPb solder, full mixing or dissolution is possible below the melting temperature of 217 °C for SnAgCu solders (Figure 4.10: d, e), assuming the time above liquidus is sufficient. The mixed SnPbAgCu liquid solder solidifies during the cooling stage of the reflow. Partially or fully mixed solder joints can form (Figure 4.10: c, d) depending on the reflow profile, SnPb/SAC ratio, and solder joint size.

If the reflow peak temperature reaches 217 °C, the SnAgCu solder ball starts melting and full mixing can be achieved for all components independent of solder joint size or SnPb paste/SAC ball ratio (Figure 4.10: g-i).

The solder joints which are not fully mixed have two distinct microstructures: the part of the SAC ball that was not dissolved and the portion that was fully mixed (Figure 4.11). The un-dissolved SAC ball structure is similar to the typical SAC alloy structure and contains primary-like Sn dendrites and Sn+Ag<sub>3</sub>Sn+Cu<sub>6</sub>Sn<sub>5</sub> ternary eutectic in the inter-dendritic spaces. The mixed solder, on the

other hand, has Sn dendrites that are much larger in size, binary Sn+Pb, ternary Sn+Ag<sub>3</sub>Sn+Pb or quaternary Sn+Ag<sub>3</sub>Sn+Pb+Cu<sub>6</sub>Sn<sub>5</sub> eutectics between the dendritic arms. In some cases, an Sn rich band is clearly visible between these two areas of the solder joint [10].

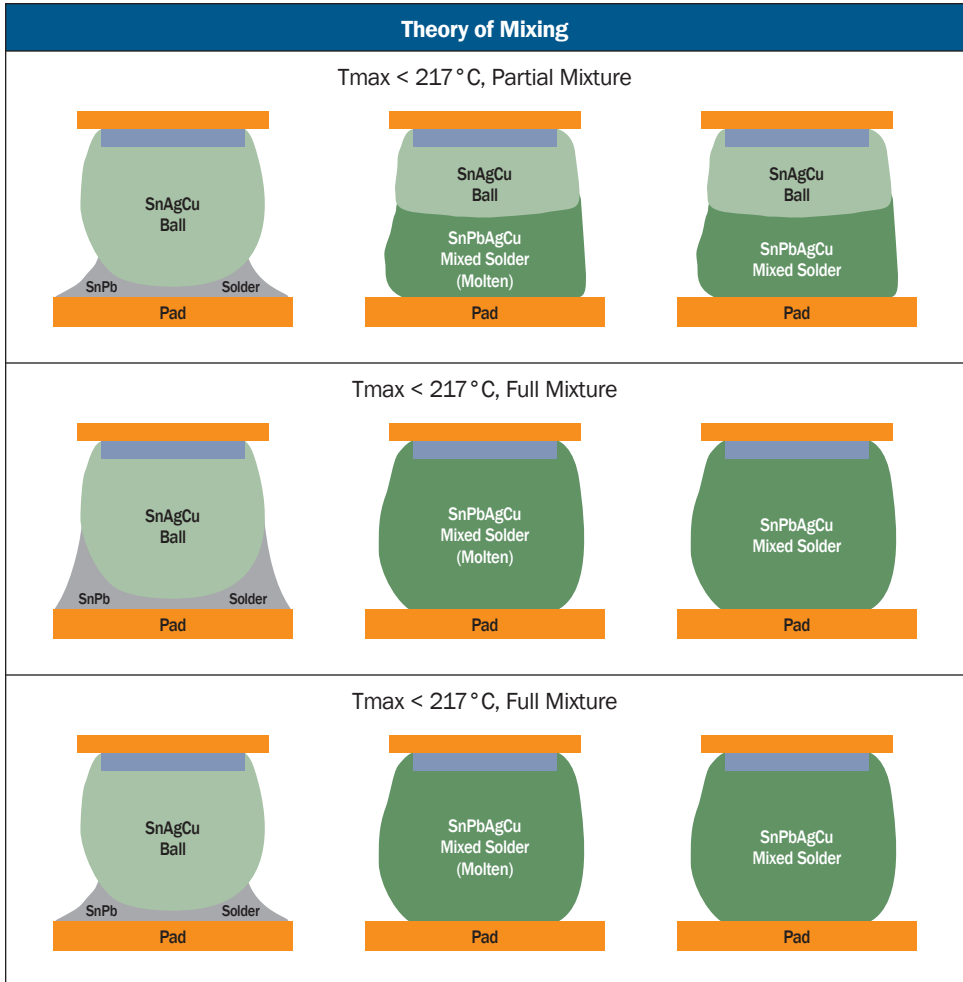
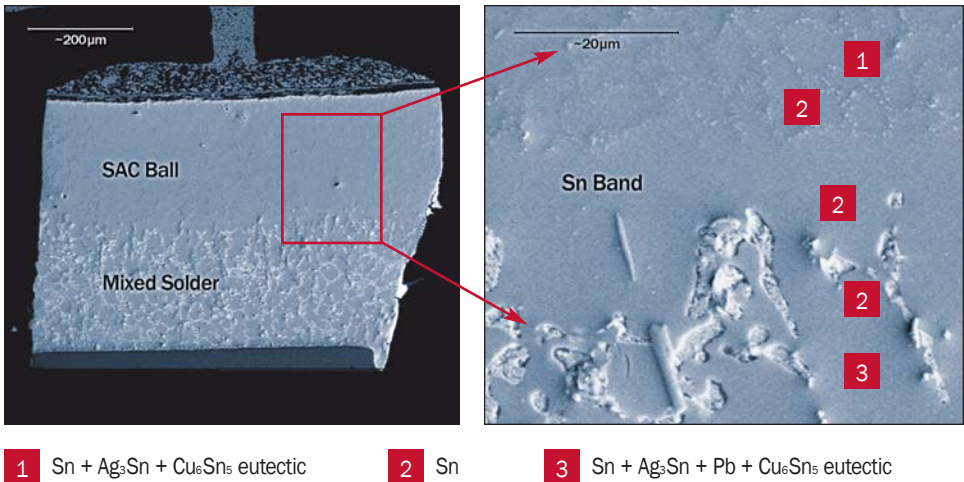


Figure 4.10 Schematic of Sn-Pb solder/SAC ball reflow metallurgy showing three possible scenarios:

- $T_{max}$  (maximum reflow temperature) below  $217^{\circ}\text{C}$ , partial mixture (a - c)
- $T_{max}$  below  $217^{\circ}\text{C}$ , full mixture (d - f)
- $T_{max}$  above  $217^{\circ}\text{C}$ , full mixture (g - i)
- a, d, g - before reflow; b, e, h - during reflow; c, f, i - after reflow [10]

#### 4. Manufacturing



**Figure 4.11** Example of a not mixed microstructure produced with peak temperature below 217 °C [4].

Fully mixed joints formed using conventional SnPb profiles and “hot” profiles have microstructures as shown in Figure 4.12 [10]. The “hot” reflow microstructure is finer than after conventional SnPb profiles. The resulting SnPbAgCu compositions have large pasty ranges. Depending on the component type, it may vary between 25 to 40 °C. Solidification in such a wide temperature range poses a high risk on the low melting phase accumulations on the board or component interface. During reflow, cooling solidification begins at the coldest location (component side during reflow) as shown in Figure 4.13. The Sn phase grows into a dendritic shape and forms toward the hot side of the board. The liquid is gradually enriched with Pb and Ag and becomes depleted of Sn, which finally crystallizes as a eutectic in inter-dendritic spaces. The last portion of liquid solidifies as a ternary or quaternary eutectic at the board side at 177 °C. Impurities that are not dissolved in solid Sn will be concentrated in the last portion of liquid (at the board side). Shrinkage voids form in the last portion of liquid as well. The interface between the intermetallic layer and solder may be insufficiently strong and may fail during thermal cycling or vibration.

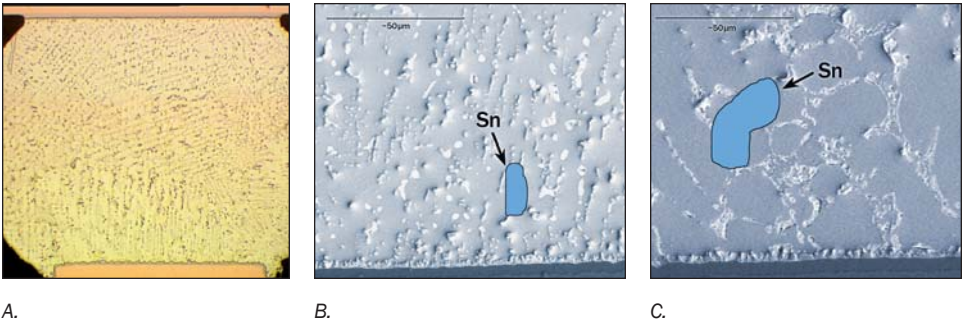


Figure 4.12 Examples of fully mixed microstructures produced with peak temperature above 217 °C (A, B) and below 217 °C (C) [4].

This area may also be secondarily melted in double sided cards during second side reflow or rework and result in shrinkage voids formation (Figure 4.14). This defect cannot be detected electrically after assembly and will reduce the field life of the product.

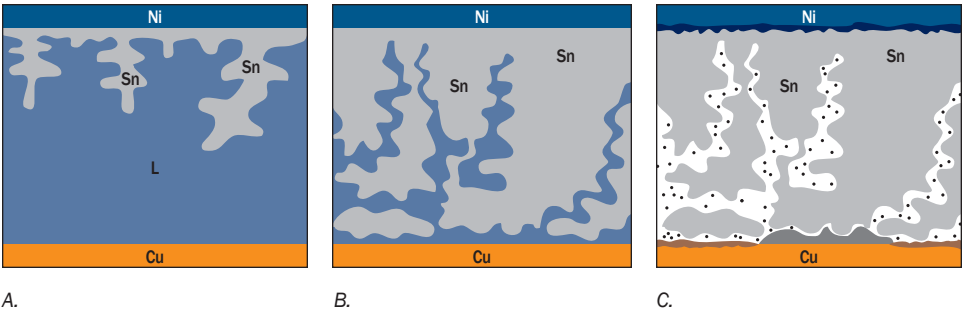


Figure 4.13 Examples of fully mixed microstructures produced with peak temperature above 217 °C (A, B) and below 217 °C (C) [4].



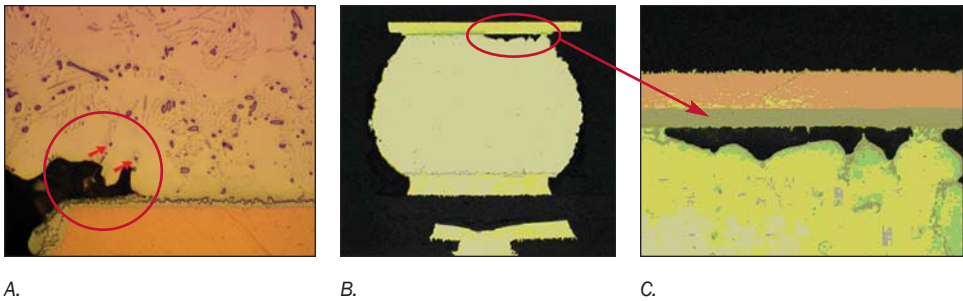


Figure 4.14 Examples of shrinkage voids forming in a eutectic SnPbAgCu (lead-enriched) zone (A) [8]; (B, C) [4].

Lead Contamination in Components With and Without Leads

Similar non-uniform Pb-enriched phase distributions may happen in components with and without leads for SnPb surface finished components in a Pb-free soldering process. This occurs under the middle of the components' leads at the solder joint/board interface, which is inevitably the area of a solder joint that results in a failure [11]. This defect cannot be detected electrically after assembly and will reduce the field life of the product.

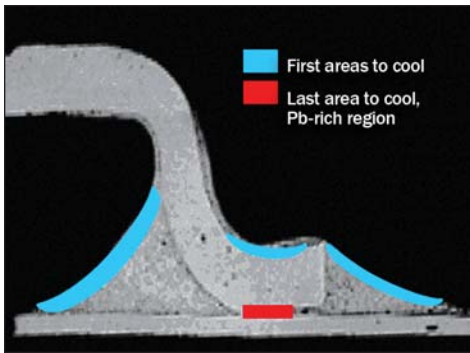
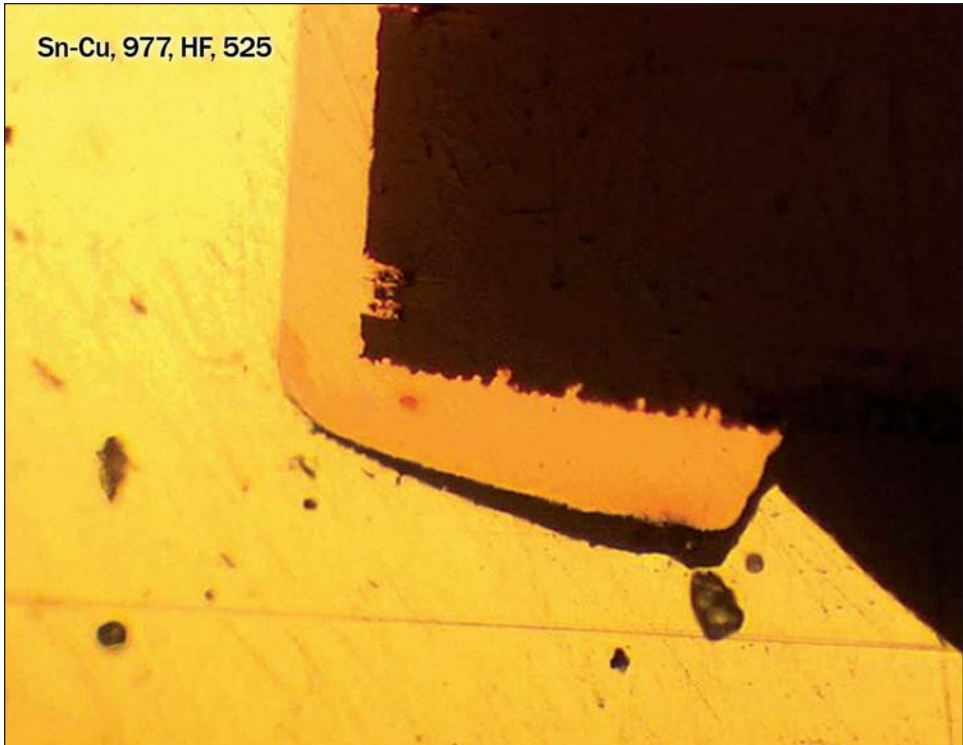


Figure 4.15 Lead contamination of solder joint for gull-wing SMT component [9].

- Fillet lift. Another phenomenon caused by a low temperature melting phase accumulation at the pad side is fillet lifting. In fillet lifting, the solder fillet lifts from the edge of the pad. Separation occurs between the intermetallic layer and the bulk solder, and it often occurs in Pb-free wave solder joints containing Bi, Pd and other additives or contaminations. It is problematic only if it causes separation of the trace.





*Figure 4.16 Fillet lift in wave solder joint. Courtesy of Celestica.*

- **Process Voids.** In addition to shrinkage voids related to the material characteristics, process related voids caused by entrapped gases are present in Pb-free solder joints. In general, SAC alloys are more prone to voiding than SnPb. The additional voids in Pb-free processes are attributed to higher processing temperatures which causes excessive oxidation of the powder. Voiding also depends on alloy composition. Off-eutectic low Ag alloys are more affected than near eutectic SAC alloy (Figure 4.17) [6].

## 4. Manufacturing

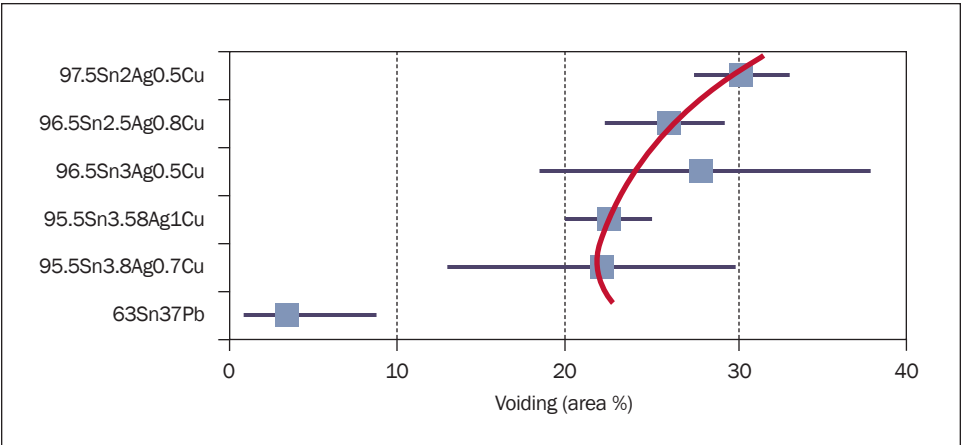


Figure 4.17 Voiding in SnPb and Pb-free alloys [6].

- Tombstone. Pb-free solder paste is more prone to tombstone failures due to higher surface tension and greater thermal gradient. The tombstoning effect is dictated primarily by melting temperature and surface tension (Figure 4.18). The further off-eutectic the SAC alloy is, the less prone to tombstoning it will be. Tombstoning can also be affected by flux chemistry and the design of the board (blind via under the discrete pad) as shown in Figure 4.19.

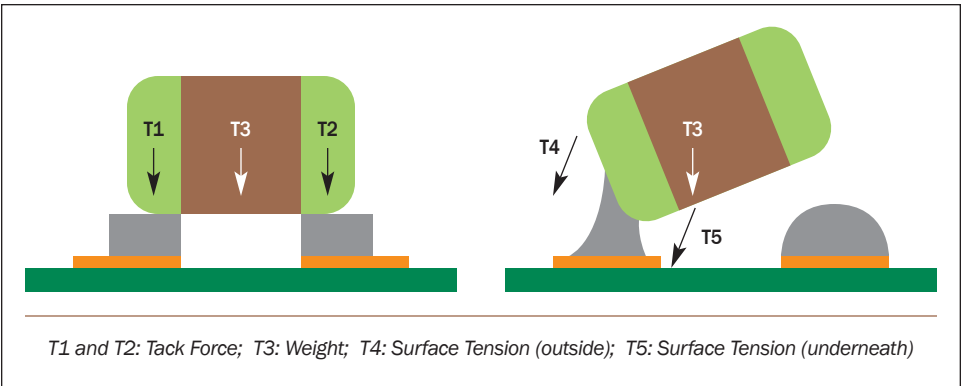


Figure 4.18 Tombstoning Defect

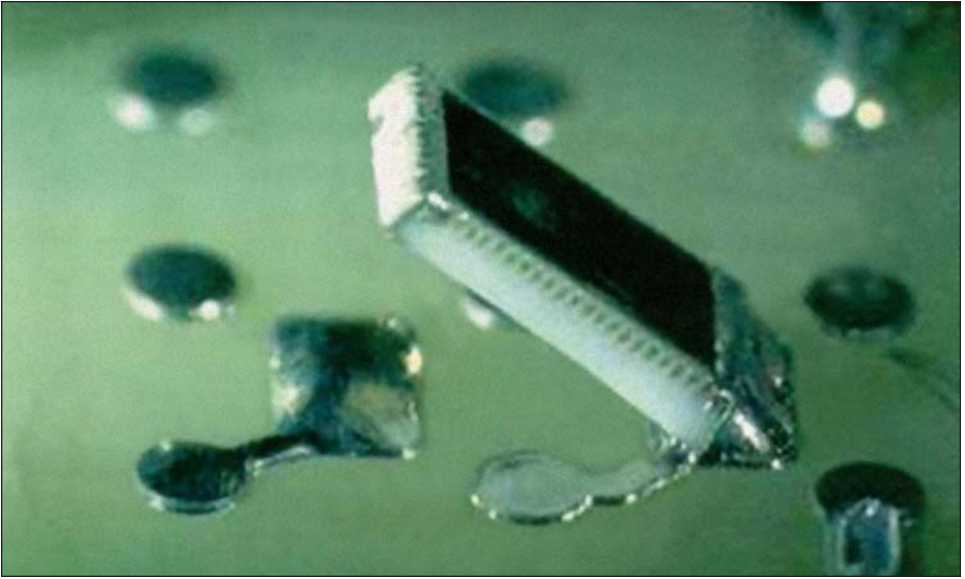


Figure 4.19 An example of tombstoning.

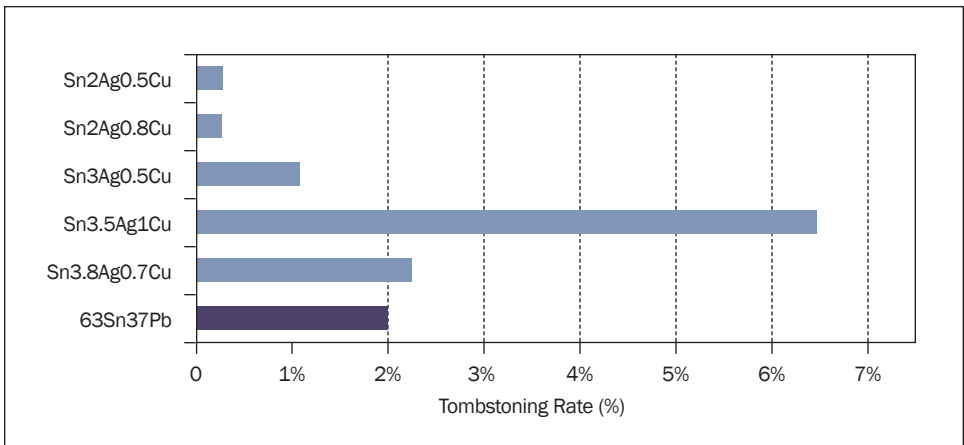
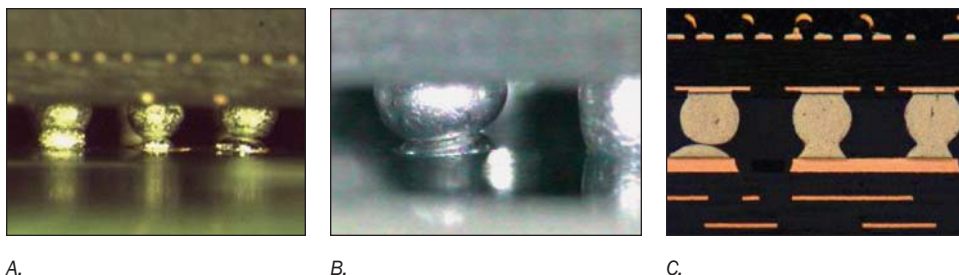


Figure 4.20 Percentage of tombstone in SnPb and Pb-free alloys comparisons [6].

## 4. Manufacturing

---

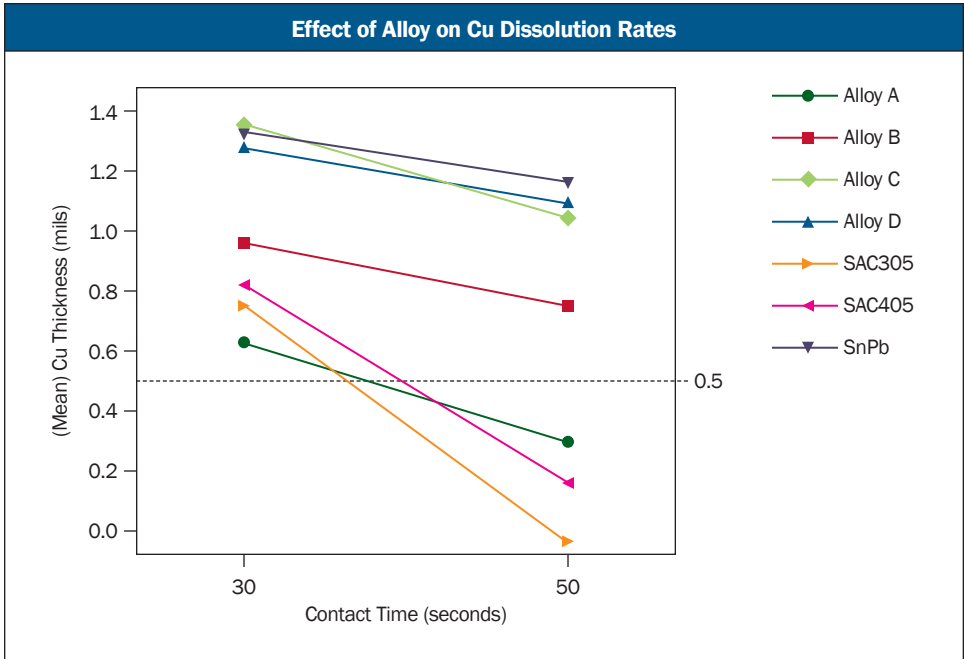
- **Head on Pillow.** Head on pillow defects occur more often in pure Pb-free and mixed metallurgy assemblies than in SnPb joints. This is attributed to the narrow process window, especially when low Ag BGA components such as SAC105 are used. The melting point of the solder balls of low Ag alloys are as much as 10 °C over the SAC305 or SAC405 ball compositions. This condition can adversely impact the assembly yields – or worse yet – create unacceptable solder joints (Figure 4.21) because the assembly was soldered at too low of a temperature. Improperly assembled components as shown in Figure 4.21 [12] are a significant reliability risk since they may pass electrical tests, but will fail more rapidly in the field than a properly formed solder joint. When a SAC ball is mixed with SnPb solder paste and the conventional SnPb profile is used, the risk of exhausting the flux is increased and the occurrence of head on pillow is also increased.



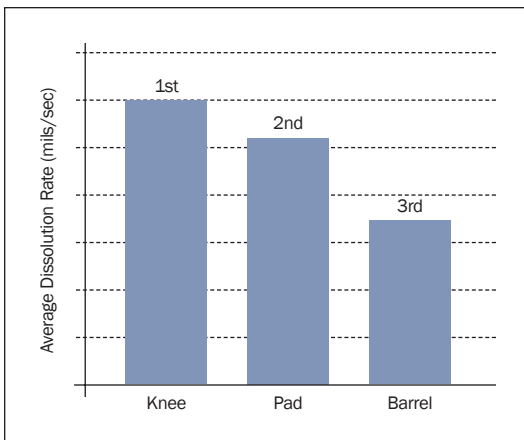
**Figure 4.21** Un-melted solder balls and unacceptable solder joints. Images A and C [10]; photo B is courtesy of Rockwell Collins.

### Copper Dissolution

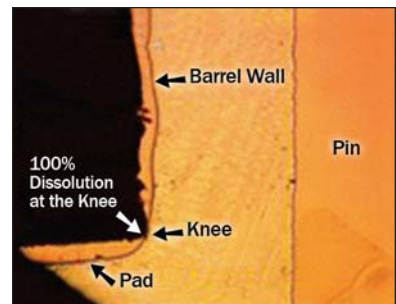
Cu plating dissolves in SAC alloys much faster than in SnPb solders (Figure 4.22). The reasons for this increase in Cu dissolution are due to the higher operating temperatures and the increase in tin content. There are a handful of alternative Pb-free alloys available on the market today which are variations of SnCu based alloys or SnCuAg alloys with low Ag content with varying degrees of elemental additives, such as Ni, Ge, Bi, Sb and others. Some alternative Pb-free alloys have been proven to make suitable replacements for highly aggressive SAC alloys during the PTH rework process [13, 14].



A.



B.



C.

**Figure 4.22** Interaction Plot Results: Effect of Alloy on Cu Dissolution Rates (A), Cu dissolution rates by barrel geometry (B), and cross-section showing 100% Cu dissolution at the knee location (C) [11, 12].

## 4. Manufacturing

---

The process issues relating to high copper dissolution rates have been well documented within the industry. The copper dissolution rates of SAC305/405 plus many of the leading alternative Pb-free wave solder alloys have been characterized and pin through hole rework process windows assessed. One remaining gap within the industry is the understanding of how the effect of Cu dissolution or thinning of the through-hole barrel wall/knee, impacts the thermal and mechanical reliability of a pin through hole joint.

### Conclusions

1. The process window for Pb-free component/Pb-free solder joint formation is very narrow compared to the SnPb process because of higher melting temperature and poorer wetting and spreading.
2. Incorporating Pb-free BGAs in SnPb solder using conventional processes may or may not allow full mixing; the resulting microstructure may not be uniform and may cause a reduction in reliability.
3. Reflow profiles with the temperature above 217 °C: the SAC solder balls melt and mix completely with the SnPb solder paste for all types of components.
4. The Pb-free microstructure is principally distinct from SnPb and consists of  $\beta$ Sn phase and hard and brittle intermetallic particles instead of two ductile solid solutions ( $\beta$ Sn) and (Pb) in SnPb resulting in dissimilar properties that behave differently over the operational life of the product.
5. Unlike SnPb, Pb-free solidification requires high undercooling and depends greatly upon cooling rate.
6. Both pure Pb-free and especially mixed metallurgy solder formation have a high propensity for low temperature phase segregation. This phenomenon is responsible for shrinkage voids and/or areas with lower strength formation.
7. Pb-free soldering is more prone to voids, tombstone, and head-on-pillow anomalies than SnPb.

8. Cu plating dissolves in SAC alloys much faster than in SnPb solders. Some alternative Pb-free alloys such as SnCuNi have a lower copper dissolution rate and have been proven to make suitable replacements for highly aggressive SAC alloys during the PTH rework process.

### Recommendations

1. The reflow, wave and rework process parameters should be carefully controlled. Temperature gradients across the board and between the components and boards should be minimized.
2. Unlike SnPb, Pb-free solidification requires high undercooling and depends greatly upon cooling rate.
3. Cooling rates in reflow, wave, and rework need further characterization to determine optimum values for reliable solder joints.
4. Components with low Ag alloys such as SAC105 should be avoided especially when used for rework.
5. Incorporating Pb-free components in SnPb assembly requires qualification for each case to choose the parameters that consistently allow complete mixing and uniform microstructure formation.
6. Alternative alloys such as SN100C should be implemented instead of SAC alloys for wave rework and probably for wave soldering to minimize copper dissolution effects.

## 4.7 SOLDER PROCESSES

### Current Baseline Practice

The following table depicts the baseline practices for soldering Pb-free in the manufacturing flow. The blocks in the flow chart are color coded to depict areas that are impacted (and to what degree) by Pb-free processing. The following section describes the details of issues and gaps for each soldering process.

4. Manufacturing

Pb-Free Processes	Manual	Reflow	Vapor Phase	Wave	Selective Wave	Selective Laser
Min. Temperature	500 °F	230 °C	230 °C	255 °C	255 °C	230 °C
Max. Temperature	700 °F	260 °C	230 °C	270 °C	270 °C	260 °C
Time Above Liquidus	2-4 sec	60-90 sec	mass driven	3-5 sec	3-5 sec	2-3 sec
Solder Bath Control						
Inert Atmosphere						
Solder Anomalies	peaks/ icicles	shrinkage voids/fillet lifting/Cu dissolution				
Equipment Changes						
Copper Dissolution						
Energy Impact						

■ No Impact    ■ Low Impact    ■ High Impact

Table 4.3 Pb-Free Solder Processes Impacts

Issues/Gaps/Misconceptions

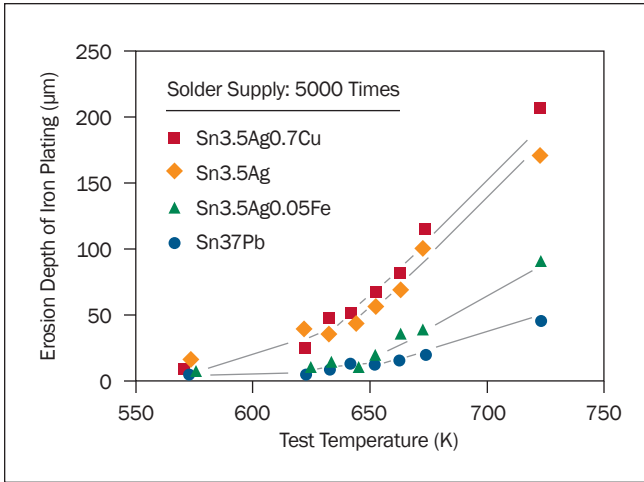
Manual Soldering

Manual soldering operations using Pb-free solder can be optimized through alteration of manual SnPb soldering procedures/equipment and by providing training (re-training) for operators who have learned manual soldering using SnPb solder. Manual soldering operators in the areas of original assembly or rework, generally require at least four hours of additional training using equipment designed for the Pb-free soldering process because of the wetting and solidification characteristics of the Pb-free solders.

A common misconception is that the same manual soldering equipment that was used for SnPb soldering can be used for the higher temperature and poorer wetting Pb-free solders. At the minimum, pre-heating hot plates and higher temperature soldering irons are recommended to do the Pb-free manual soldering.

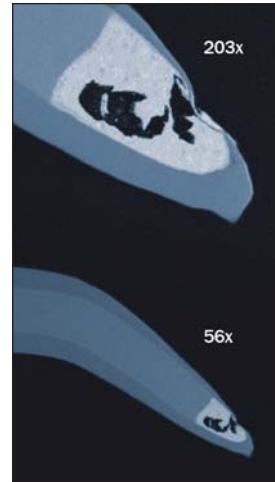
New Pb-free optimized soldering irons and tools such as hot air pens are available to improve the effectiveness and quality of manual soldering on the Pb-free electronics product.





Effect of test temperature on erosion depth of iron plating in several solders after 5,000 solder applications.

A.



B.

Figure 4.23 Impact of Manual Pb-Free Soldering Process on Soldering Iron Tips. A [1]; B [2].

### Reflow Soldering

The implementation of Pb-free solder has a major impact on the reflow soldering process. The impact on the reflow equipment falls into two major categories: equipment configuration and energy costs.

- Equipment Configuration:
  - Thermal profiling concerns: In accordance with good manufacturing practices associated with SnPb profiling, a sufficient number of thermocouples need to be strategically placed in various areas across the top and bottom sides of the CCAs. The higher reflow temperatures associated with Pb-free may cause a greater thermal gradient across the assemblies that will require additional thermocouples for a more accurate temperature profile.
  - Pb-free solder alloys melt at 217 °C, which is an increase of 34 °C from conventional SnPb solder alloys. Reflow ovens should have a minimum of seven reflow zones to adequately cover the increased thermal input demands of the Pb-free solder alloys. Reflow ovens utilizing fewer reflow zones may result in issues in solder joint formation. The use of an inert atmosphere will result in a larger reflow process window and solder joint visual characteristics. The use of an inert atmosphere is not required but is highly recommended.

## 4. Manufacturing

- **Energy Costs:** Industry studies have documented that the use of Pb-free SAC solder alloys in the reflow process results in increased energy consumption (Figure 4.24) when compared to the use of SnPb solder alloys [15].

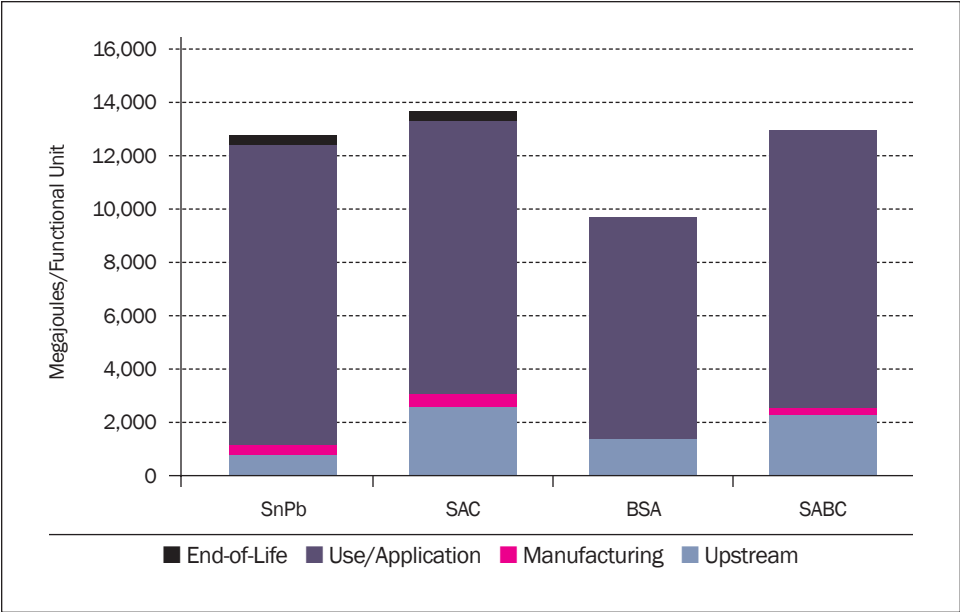


Figure 4.24 Reflow process energy consumption comparison [15].

- **Thermal Profile:** The change in the solder alloy melting temperature due to the implementation of Pb-free solder has a direct impact on the reflow process profile. Component maximum temperature limits (Section 3.4.1, Design for Manufacturing) and the increase in solder alloy melting points result in a very restricted reflow profile (Figure 4.25). The electronics industry is currently investigating the necessity of implementing a controlled cooling rate requirement for CCA solder reflow processes.

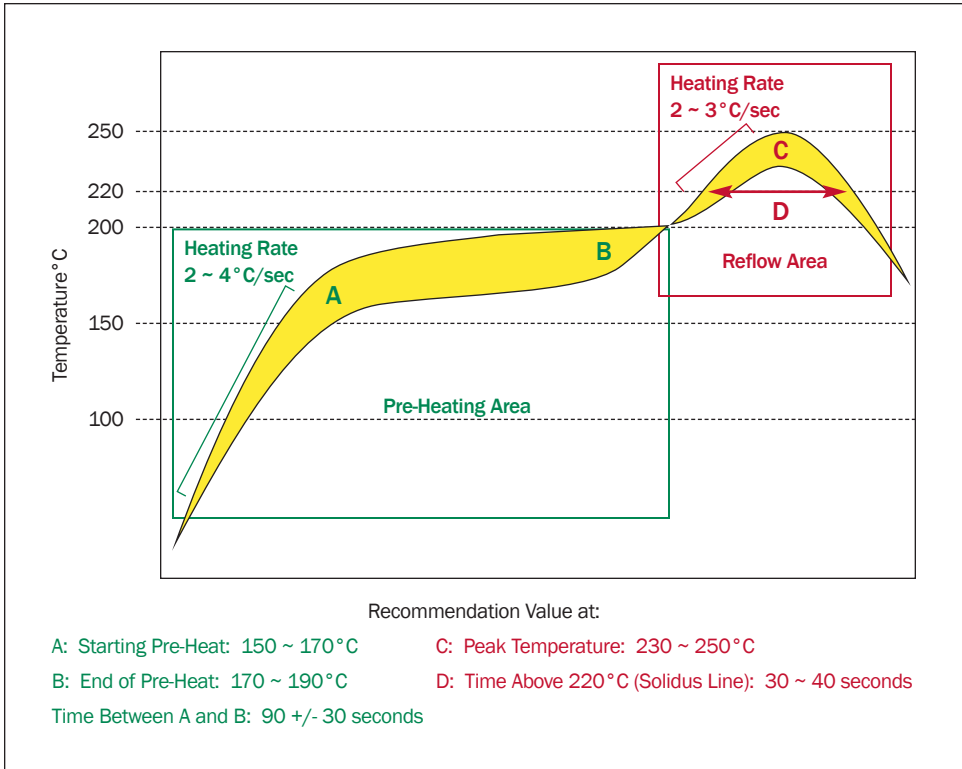


Figure 4.25 Reflow Solder Profile

#### Wave Soldering

The implementation of Pb-free solder has a major impact on the wave soldering process. The impact on the reflow equipment falls into three major categories: equipment configurations, energy costs, and solder bath control.

- **Equipment Configuration:** The Pb-free solder alloys are tin rich in composition. Molten tin has very aggressive dissolution and erosion characteristics. The traditional wave solder equipment contained a variety of components (fabricated from cast iron and/or stainless steel) which had poor compatibility with molten tin (Figure 4.26) [10, 16]. The use of Pb-free solder alloys which contain specific elemental additions to regulate dissolution/erosion can also be employed to address the wave solder equipment damage concerns.

## 4. Manufacturing

The use of wave solder equipment fabricated from titanium, with molten tin resistant coatings, or specific Pb-free solder alloys that cause minimum equipment damage, is recommended. The use of an inert atmosphere will result in a larger wave solder process window and improved solder crossing characteristics. The use of an inert atmosphere is not required but is highly recommended.

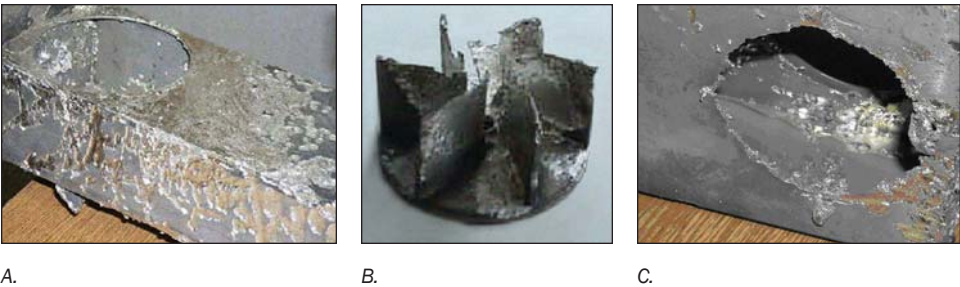


Figure 4.26 Wave solder equipment damaged by Pb-free solder [10, 16].

- Energy Costs: Industry studies have documented that the use of Pb-free SAC solder alloys in the wave solder process result in increased in energy consumption (Figure 4.27) when compared to the use of SnPb solder alloys [17].

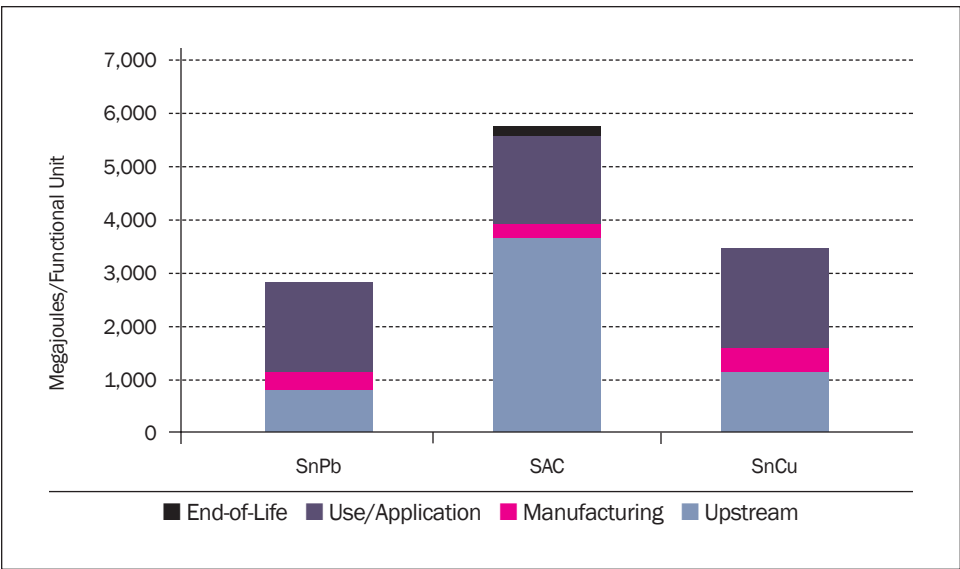


Figure 4.27 Wave solder process energy consumption comparison [17].

- Solder Bath Control:** The electronics industry has traditionally assessed/monitored the level of solder bath contamination in accordance with the requirements of ANSI-JSTD-001 for SnPb solder alloys. Although a number of commercial electronic manufacturing facilities have been running Pb-free wave solder processes, minimal assessment data exists for the various Pb-free wave solder baths and no industry consensus requirements exist.
- Thermal Profile:** The implementation of Pb-free solder has a direct impact on the wave solder profile and parameters. The increased solder alloy melting point results in an increase in the wave solder profile requirements (Figure 4.28). It is recommended that the maximum amount of preheating capability be utilized for the wave solder equipment. Additionally, the wave solder flux supplier process controls, handling, storage and equipment parameters for the specific flux product should be followed. The electronics industry is currently investigating the necessity of implementing a controlled cooling rate requirement for CCA wave solder processes.

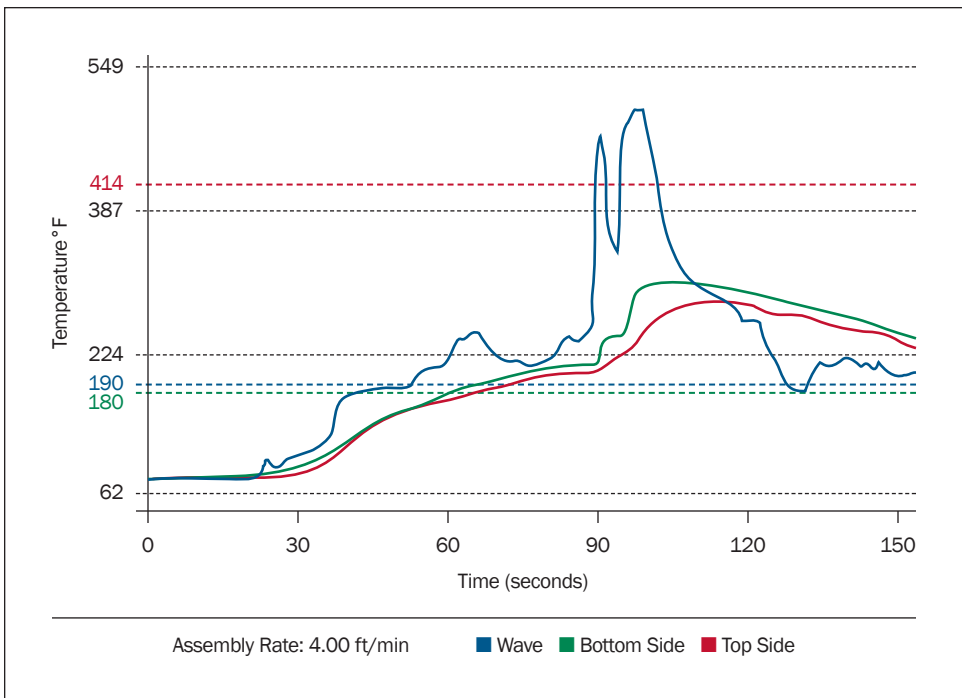


Figure 4.28 Pb-free Wave Solder Profile. Courtesy of Celestica.

## 4. Manufacturing

### Vapor Phase Soldering

The impact of the Pb-free soldering process on the vapor phase soldering process is minimal. The use of existing vapor phase equipment with Pb-free solder will require a change in the vapor phase solder process chemistry. The melting point of the Pb-free solder alloys is higher than the traditional 215°C boiling point chemistry. Pb-free vapor phase equipment will require a 230°C boiling point chemistry and the associated changes in the equipment temperature sensors/controls. It is also recommended that the vapor phase cooling coil module be assessed for efficiency. The thermal mass of the CCA will determine if any changes in the vapor phase process profile are required.

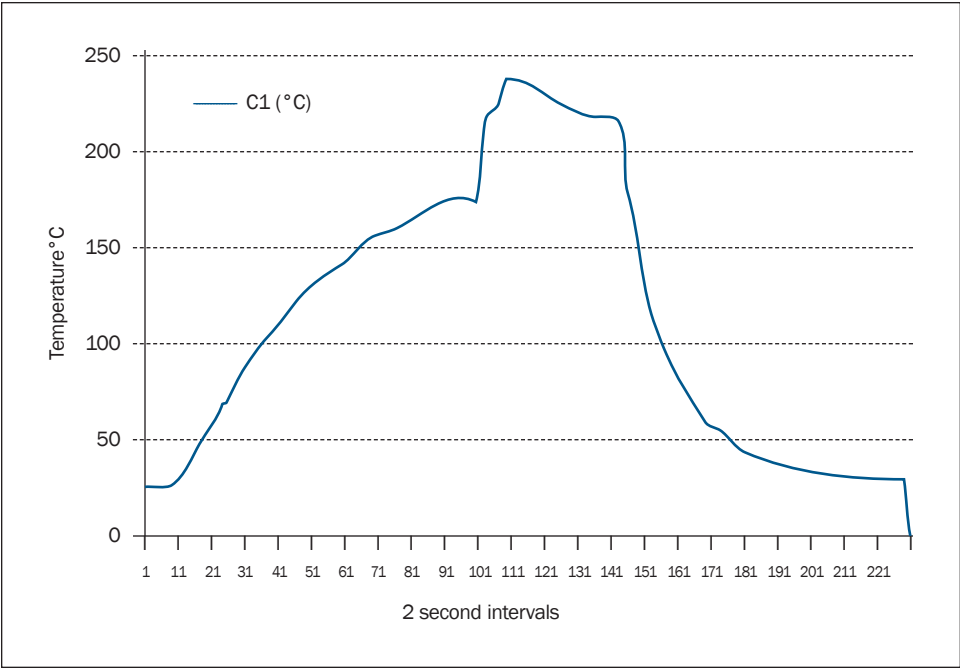


Figure 4.29 Typical vapor phase thermal profile using a 240°C fluid. Courtesy of Solvay Solexus.

### Selective Soldering

This soldering process is used to perform secondary solder operations for components that are soldered after the mass reflow or wave solder processes. This is typically for parts not capable of mass soldering processes due to temperature sensitivities or geometry (connectors with through pins or surface mount over the card edge and hardware installed).

There are two common methods for selective soldering: solder pot wave type process and the laser soldering process. Both can be automated and equipment is available for these processes. Proper equipment specification is required to ensure the higher temperatures can be met. Additionally, the solder pot type equipment must specify materials that are compatible to the Pb-free solders. Laser diode power must be selected to meet higher processing temperatures and processes should be developed to ensure adequate reflow without board laminate damage (Figure 4.30).

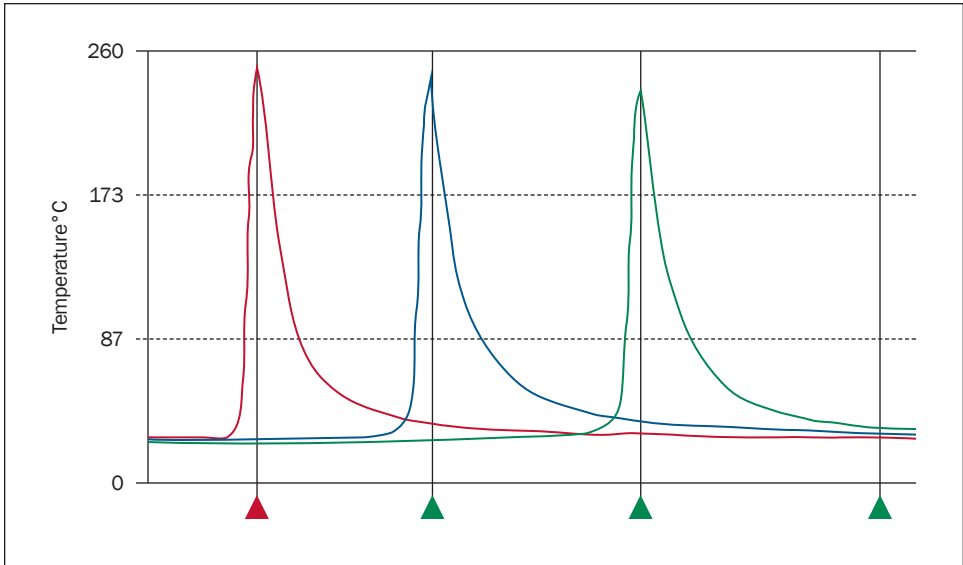


Figure 4.30 Laser Solder Thermal Profile. Courtesy of Lockheed Martin.

### Conclusions

The SnPb processes and equipment for soldering can be used with modifications for transitioning to a Pb-free soldering process. Additional cost for equipment upgrades and energy consumption will be realized.

### Recommendations

- Ensure the equipment and processes used for Pb-free soldering are thoroughly evaluated for materials capability and the increase in temperature.
- Process development characterization and qualification will be required.
- Manual soldering operators should undergo a minimum of four hours of additional training using equipment designed for the Pb-free soldering processes.

## 4. Manufacturing

---

- Pre-heating hot plates and higher temperature soldering irons are recommended (as necessary) process aids for Pb-free manual soldering processes.
- An assessment of soldering irons and tools should be conducted to determine if new equipment is necessary and/or a periodic maintenance schedule needs to be established.
- Reflow ovens should have a minimum of seven reflow zones to adequately cover the increased thermal input demands of the Pb-free solder alloys.
- The use of an inert atmosphere is not required but is recommended.
- The use of wave solder equipment fabricated from titanium, with molten tin resistant coatings, or specific Pb-free solder alloys that cause minimum equipment damage, is recommended.
- The use of an inert atmosphere, which will result in a larger wave solder process window and improved solder dressing characteristics, is recommended.
- It is recommended that the maximum amount of preheating capability be utilized for the wave solder equipment.
- It is recommend that additional resources be dedicated to investigating the necessity of implementing a controlled cooling rate requirement for CCA wave solder processes.
- Minimal assessment data exists for the various Pb-free wave solder baths on acceptable elemental contamination values, and it is recommended that further investigation on the issue be conducted.
- Pb-free vapor phase equipment will require a 230°C boiling point chemistry and the associated changes to the equipment temperature sensors/controls.
- Laser diode power for laser soldering processes must be selected to meet higher processing temperatures and processes should be developed to ensure adequate reflow without board laminate damage.

### 4.8 DEPANELING/ROUTING

#### **Current Baseline Practice**

Depaneling/routing of circuit card assemblies from panels can be done either using mechanical routing bit processes or non-contact laser processes. Laser processes are still in the development stage and are considerably more costly.



### Issues/Gaps/Misconceptions

Damage to solder joints during the routing process is a major concern. Mechanical routing can cause damage to solder joints by stresses induced in the joints during the cutting process. Mechanical routing of SnPb circuit cards is performed regularly and design rules are employed to prevent placing components too close to the edge of the circuit cards where the actual cutting will take place. Pb-free solder joints are typically more brittle than SnPb joints and therefore more susceptible to damage during this process.

### Conclusions

Laser equipment is non-contact and therefore allows for closer placement of parts to the card edge; however, other damage from the laser heat must be considered, and the equipment is very costly. Mechanical routing will require new design rules be established to determine how close solder joints may be placed to the cutting area without causing joint damage.

### Recommendations

Careful process qualification must be employed for either laser or mechanical routing to determine the most suitable method to remove the CCA from the panel. Consider the design and placement (proximity to the edge of the circuit card) of the components as well as the cost of the equipment to perform this task.

## 4.9 CLEANING

### Current Baseline Practice

Cleaning processes and equipment have been developed and tested thoroughly for SnPb fluxing systems. Pb-free fluxes will need to be tested and qualified to ensure compatibility with the product being cleaned. No clean Pb-free systems require additional qualification to ensure remaining fluxes have been fully activated and leaving them on the product will not cause long term failure.

### Issues/Gaps/Misconceptions

Inadequate cleaning practices can cause severe failures during the product's life cycle. Pb-free fluxes are more difficult to remove due to the increased temperature during the soldering process. Current high density low standoff electronics designs add complexity to the cleaning process development. Current resistivity of solvent extracts testing is not capable of penetrating and removing residues under low component clearances and results could be misleading.

## 4. Manufacturing

---

### Conclusions

A Pb-free cleaning process can be established using current cleaning chemistries and equipment, provided an extensive evaluation is performed including testing for contaminants remaining after cleaning.

### Recommendations

Perform a thorough cleaning process evaluation including testing for contamination after cleaning. Ensure the cleaning chemistries are compatible with all materials in the product to be cleaned. Compatibility must be shown between all adhesives, conformal coatings, and any other materials. Removal of low standoff parts during process development is recommended to ensure all flux residues have been removed.

## 4.10 UNDERFILL PROCESS

### Current Baseline Practice

The implementation of Pb-free solder processes has no impact on the application and use of underfill materials on CCAs. The electronics industry traditionally utilizes underfill materials to provide additional solder joint integrity in cases where the use environment has vibration or shock demands (Figure 4.31). Underfills can cause early thermal cycle failures if coefficient of thermal expansion (CTE) is not closely matched.

### Issues/Gaps/Misconceptions

The underfill material supplier's process controls, handling, storage and equipment parameters for the specific underfill product should be followed. No changes in underfill application methodology are required. Underfill materials have also been utilized in some design situations to provide enhanced solder joint integrity of Pb-free area array components (e.g., BGAs, CSPs, and FCs).

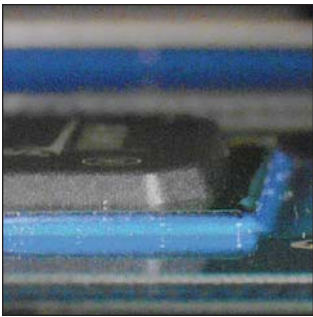
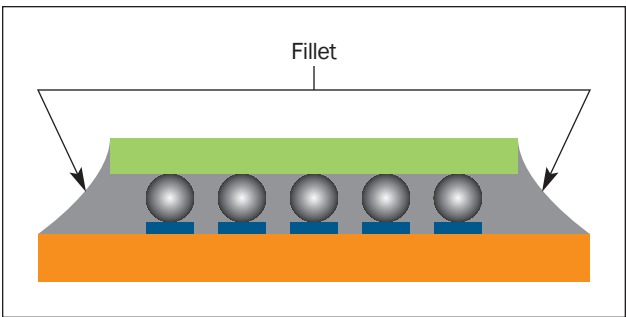




Figure 4.31 A BGA component utilizing underfill. Courtesy of Rockwell Collins.

### Conclusions

The implementation of Pb-free solder processes has no impact on the application and use of underfill materials on CCAs processes.

### Recommendations

Not applicable.

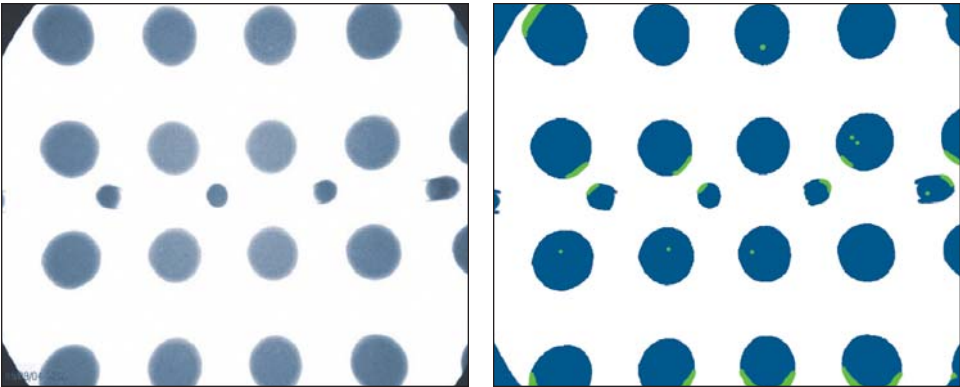
## 4.11 INSPECTION PROCESSES

### Current Baseline Practice

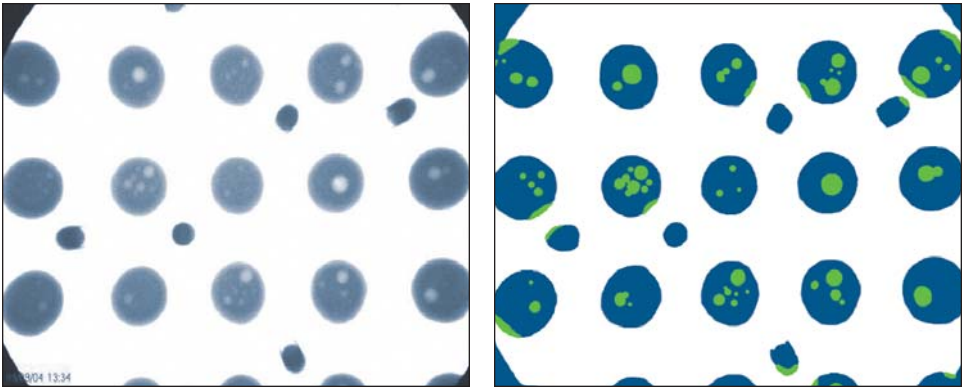
Inspection processes and equipment have been well established for SnPb solder inspection. Pb-free inspection techniques are being adopted into IPC specifications [18] demonstrating visual inspection requirements, while automated equipment continues to develop new techniques for inspecting Pb-free solder joints.

Issues/Gaps/Misconceptions

The implementation of Pb-free soldering processes will have a direct impact on the manufacturing inspection processes. The electronics industry utilizes the IPC-A-610D for CCA visual inspection workmanship requirements [18]. Pb-free soldering processes have additional solder defects in comparison to SnPb solder defects. The visual appearance of acceptable Pb-free solder joints can have visual characteristics such as a dull, matte finish and rougher surface texture. Additional Pb-free solder defects and visual acceptance criteria requirements need to be developed for inclusion in the IPC-A-610D specification. It is also recommended that CCA inspection personnel undergo additional Pb-free solder manual process training, and Pb-free workmanship standards training to assist in the implementation of a Pb-free soldering process. Automated inspection technologies such as automated optical inspection (AOI) or automated x-ray inspection (AXI) will require some changes in equipment parameters (e.g., lighting techniques) and revision of inspection algorithms. The current equipment parameters and inspection algorithms may not adequately identify solder defects, resulting in false negative/false positive characterization of CCA solder joints. Finally, industry testing has shown that Pb-free soldering processes tend to produce more solder joint voiding anomalies; thus, AXI algorithms will require review and possible revision. Figure 4.32 illustrates the increased voiding phenomenon.



A. SnPb X-Ray Image and Voiding Analysis



B. Pb-Free X-Ray Image and Voiding Analysis

*Figure 4.32 X-ray image comparing SnPb (A) and Pb-free (B) solder joint voiding anomalies. Images are courtesy of JCAA JGPP No Lead Consortia Project.*

### Conclusions

Current algorithms and equipment parameters (e.g., lighting) may not adequately identify defects in Pb-free solder joints.



*Figure 4.33 Visual comparison of SnPb versus Pb-free solder joint. Courtesy of Henkel Loctite.*

### Recommendations

Additional Pb-free solder defects and visual acceptance criteria requirements need to be developed for inclusion in the IPC-A-610 specification. CCA inspection personnel need to undergo additional Pb-free solder manual process training and Pb-free workmanship standards training. Automated inspection technologies will require some changes in equipment parameters (e.g., lighting techniques) and revision of inspection algorithms.

### 4.12 REWORK

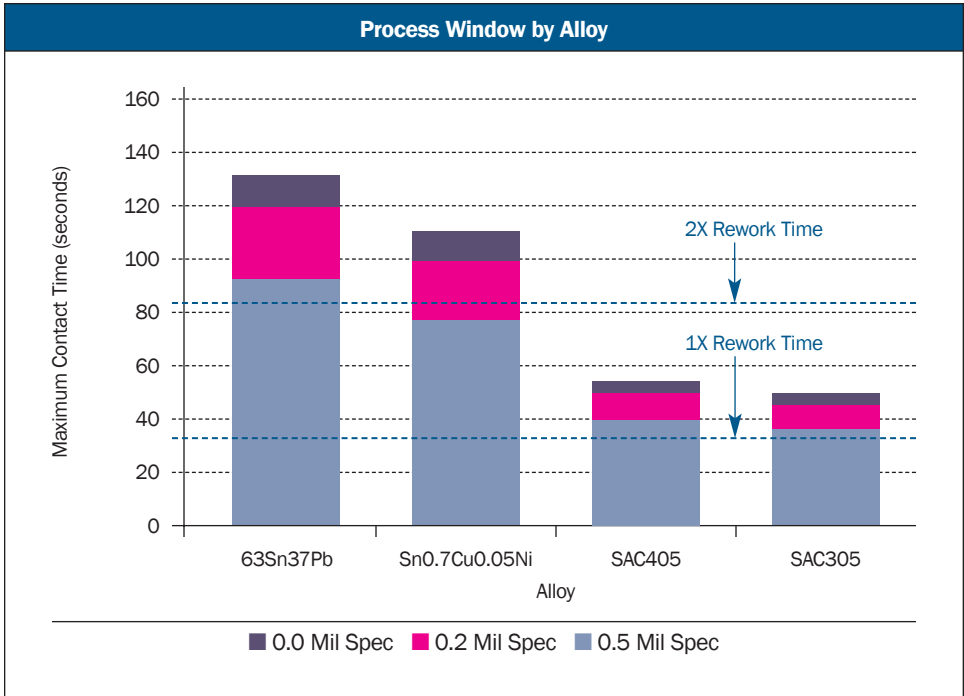
#### Current Baseline Practice

SnPb rework processes and equipment are well established including hot air, fountain wave solder, and manual rework. The Pb-free hot air rework and fountain wave solder are the most challenging processes in Pb-free rework procedures. Additional equipment improvements and qualification will be needed for the transition to Pb-free assembly rework.

#### Issues/Gaps/Misconceptions

The techniques used for Pb-free rework are dramatically different from SnPb based techniques.

- Hot air rework:
  - In pure Pb-free, CCA preheat temperature is higher than with SnPb processes.
  - Preheat should be increased (up to 15 minutes dependent upon thermal mass).
  - The board damage such as warpage and pad cratering may be an issue.
  - Thick intermetallic formation may cause reduced reliability.
  - Insufficient flux activation in double sided assembly may cause dendritic growth.
  - In mixed assembly, high temperature gradient and uneven solidification may lead to an interfacial fracture.
  - Hot air rework equipment must be capable of preheating to a 120°C minimum.
- Fountain rework:
  - Cu dissolution may occur when using SAC305 Pb-free fountain based rework after only one rework cycle (Figure 4.34).
  - During the initial manufacturing process, utilization of SnCu modified alloys, such as SN100C, will minimize the degree of Cu dissolution during subsequent rework.
- Manual rework (repair):
  - Soldering iron wear is a danger with Pb-free manual soldering.
  - Operator training is required to upgrade manual soldering techniques for Pb-free.
  - A dedicated Pb-free work station is recommended.



**Figure 4.34** The impact of solder alloy selection on the copper dissolution rate during PTH rework.

## Conclusions

Rework processes can be qualified for Pb-free assemblies with proper consideration of equipment selection and process thermal profile development.

## Recommendations

A complete re-qualification of the rework process and procurement of rework equipment capable of maintaining the higher temperatures required for Pb-free rework is required. Preheat should be carefully considered in order to ensure uniform and constant heat to the assembly and to reduce thermal shock of the PCB and components.

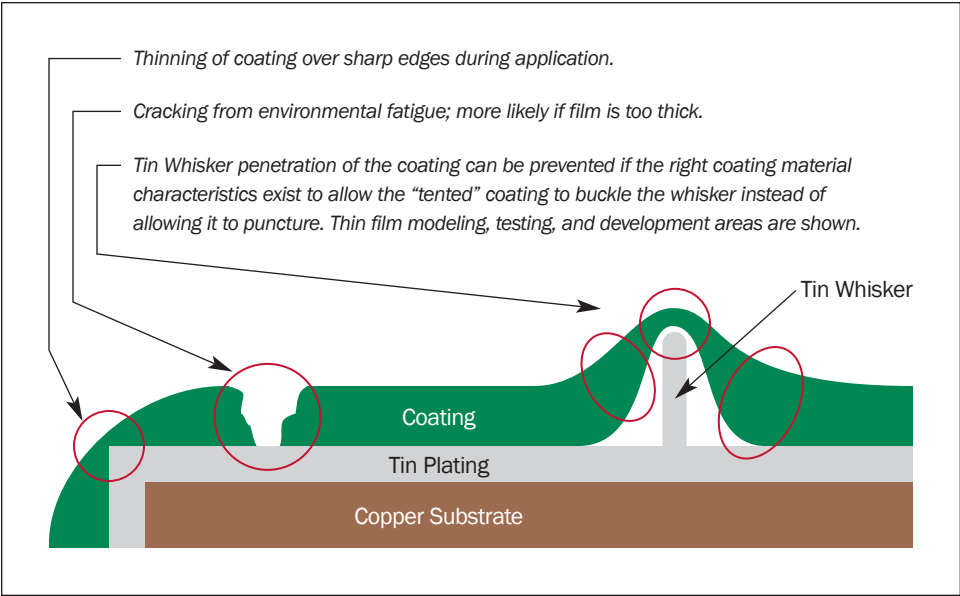
4.13 CONFORMAL COATING

Current Baseline Practice

SnPb circuit card assembly conformal coating processes utilize several methodologies including hand spray, dip, semi-automatic, and fully automatic. Automated process equipment is very mature, and selective coating machines are capable of applying complete coating coverage to a desired thickness, without the need to mask off areas that are to be free of coating.

Issues/Gaps/Misconceptions

The industry’s conformal coating processes will be relatively unchanged by the implementation of Pb-free solder processes. Traditionally, conformal coating has been utilized in CCA designs as a method to inhibit the intrusion of moisture and as a debris barrier [19]. The use of pure tin surface finishes has introduced a new CCA failure mode – tin whiskers (Section 7.2, Failure Sources). Conformal coating is considered by the industry to be one segment of an overall tin whisker risk mitigation protocol [20]. The conformal coating type, process parameters (thickness, quality of coverage, etc.), and the inspection of conformal coating will require changes for applicability as a tin whisker risk mitigation practice. Tin whisker mitigation effectiveness of each conformal coating type needs to be better documented, particularly the those more recently developed that are formulated specifically for tin whisker mitigation purposes.



A.





B.

*Figure 4.35 The containment of tin whiskers by conformal coating. Diagram A is courtesy of Bob Ogden, Raytheon; photo B is from ACI Technologies, Inc.*

### Conclusions

Current industry conformal coating processes will need to undergo minor changes due the implementation of Pb-free soldering processes. These minor changes relate to the increased process control parameters and inspection requirements dictated by the use of conformal coating in tin whisker risk mitigation protocols. Newly developed whisker mitigating coatings need to be fully characterized and qualified for use.

### Recommendations

It is recommended that the CCA producer establish objective evidence demonstrating conformal coating process control parameters and inspection requirements pertinent to the use of conformal coating in tin whisker mitigation protocols.

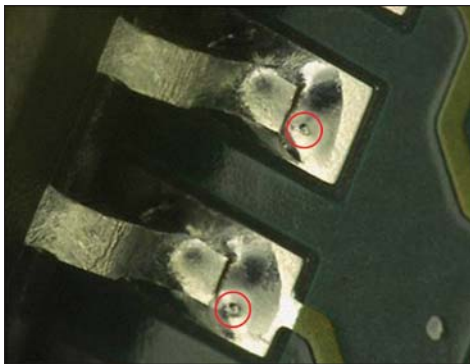
4.14 TEST

Current Baseline Practice

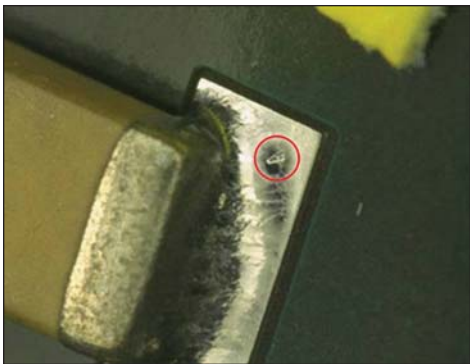
Equipment is available for probe type testing of networks and some component value measurements for products on the manufacturing line. This equipment is referred to as “flying probe” testers. These testers allow for fixtureless testing as a replacement to the traditional “bed-of-nails” type contact testers which required dedicated fixtures for each product. Additional functional level testing is performed to find manufacturing process defects. Typically, these tests are ESS tests used to ensure long term reliability of the product.

Issues/Gaps/Misconceptions

The implementation of Pb-free solder processes has a significant impact on the testing of CCAs. Industry data has demonstrated that the Pb-free alloy CCAs are more prone to bending induced damage than the current SnPb alloy CCAs. Defects such as pad cratering, circuit trace cracking and plated through-hole damage can result due to the bending/warping induced by bed-of-nails, flying probe, and other types of test systems. An assessment of the handling, mounting, and test fixture protocols should be conducted to determine if there is any potential of inducing CCA damage. Probe testing also requires a probe to touch solder joints which can leave an impact mark on the joint (Figure 4.36). Pb-free joints are more brittle than SnPb joints, and therefore the impact of the probe could cause more damage to the joint, and must be be assessed to determine if the damage causes long term reliability concerns.



A.



B.

*Figure 4.36 Image A shows probe marks on solder joints and image B indicates a probe mark on pad away from solder joint. Photos are courtesy of Lockheed Martin.*

### Conclusions

The functional and process quality CCA testing is significantly impacted by the implementation of Pb-free solder processes and additional evaluation must be conducted.

### Recommendations

An assessment of CCA handling and fixture protocols needs to be completed prior to the testing of Pb-free CCAs. Assessment of the impact of contact probing must also be assessed. When possible, programming the probe tester to impact the pad away from the solder joint is desirable (Figure 4.36).

## 4.15 PACK AND SHIP

### Current Baseline Practice

SnPb circuit card packing and shipping practices are adequate for Pb-free.

### Issues/Gaps/Misconceptions

None.

### Conclusions

There is no change to the pack and ship procedures when dealing with Pb-free assemblies.

### Recommendations

Some consideration for handling of Pb-free circuit cards is recommended. Handling precautions are discussed in Section 4.2, Design for Manufacturing; specifically, *Printed Circuit Boards* and *Manufacturing Personnel Training*.

“We can lick gravity, but sometimes the paperwork is overwhelming.”

—Wernher von Braun (1912-1977)



# 5. Sustainment

## 5.1 INTRODUCTION

Sustainment often is understood to include provisions for end-of-life of a given project, for which there currently exists a large body of knowledge, legal requirements, industry policies, processes, and practices. The existing system adequately addresses end-of-life issues. The same organizational structure can be used for addressing Pb-free issues with a greater emphasis on ensuring that the proper metrics that compose a good sustainment process be followed rigorously to ensure compliance. Appropriate control of parts and processes to mitigate the uncertainty introduced by the insertion of Pb-free electronics into systems will require additional effort.

The transition to Pb-free electronics will have a profound impact on sustainment of A&D systems. Configuration control and reliability risks will rise to unacceptable levels if not understood as urgent, and managed appropriately. Those risks are driven by unique A&D requirements including:

- Long product service lifetimes.
- Rugged operating environments.
- High consequences of failure.
- Repairability at the circuit card assembly level.

If the number of solder alloys used in original assemblies proliferates, a lack of proper product identification and configuration control will result in product reliability and potential failure risks. The processes for identification of the alloys used in original assemblies will likely require enhancement, particularly for support of repair procedures, to manage these risks. The risks will increase exponentially as the number of available solder alloys and part finishes increases. In consideration of the fact that each repair facility must deal with products from scores of hardware manufacturers, and that each hardware manufacturer may choose from multiple assembly solder alloys, the potential proliferation of alloy combinations will be unacceptable, unless tighter controls are put in place to define the acceptable alloys for reworking.

Reliability risks will result if the alloys used to repair an assembly have not been qualified, verified, and documented as compatible with the alloys used for original manufacture.

In addition to the above risks, there is an enormous potential for increased life cycle cost. It is critical for the feedback loops among repair facilities, hardware design authorities, and manufacturing activities be significantly improved to accommodate Pb-free electronics. This improvement is possible in commercial A&D operations, but systemic disconnects exist in military operations, because the contracts for repair, production, and support are rarely connected. Comprehensive industry implementation of Pb-free Control Plans, verified as compliant to GEIA-STD-0005-1[1], can facilitate the realization of these goals.

5. Sustainment

The Sustainment section of this report will describe the current baseline practices as they exist for Pb-free in the areas of Configuration Management (CM), Logistics, and Repair. What will become apparent during the dissemination of these procedures, are the noticeable gaps, issues, and misconceptions surrounding the current practices. The report will also include conclusions from the assessments of these practices, and recommended actions to mitigate the impact on the sustainment efforts directed toward Pb-free electronics.

The Sustainment Sphere of Influence

The flow chart in Figure 5.1 illustrates the interrelationships and scope of how the various elements of the sustainment process interact within a program management structure. From the flow chart, it can be ascertained that manufacturing, design, reliability and test play a critical role in influencing product life cycle.

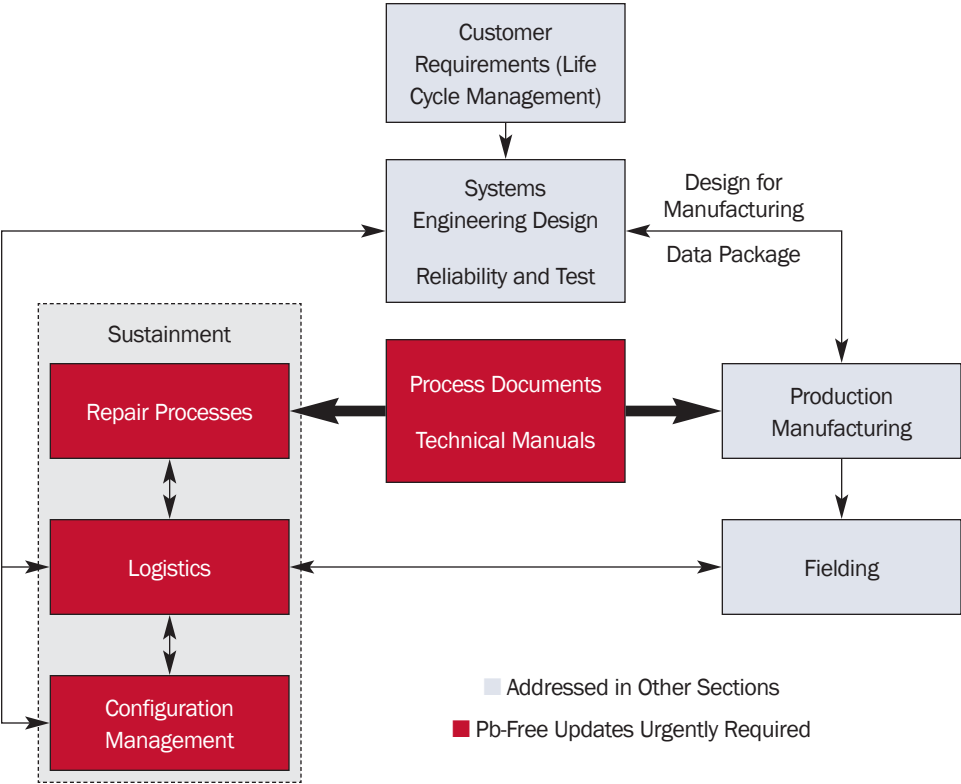


Figure 5.1 Sustainment Impact. Introduction of Pb-free materials and processes will require significant changes in sustainment practices.

Because of the large number of interactive areas, all with issues around Pb-Free, the probability of a latent manufacturing, design, or reliability problem manifesting itself and subsequently affecting the sustainment process, increases dramatically. The potential for increased reliability risk, due to configuration control issues, may coerce OEM's to consider extraordinary and often costly measures previously regarded as unnecessary, or too expensive. An example of a preventative measure may be:

- Limiting the number of assembly alloys used in product design, which can increase cost.
- Designing disposable electronic assemblies, which may be suitable for commercial applications, but not always an option for A&D applications.

## 5.2 CONFIGURATION MANAGEMENT

### Current Baseline Practices

The A&D configuration management process is mature, follows well defined and current industry standards, includes vertically and horizontally cross-functional elements, and is critical to the control of product life cycle costs and sustainment. Configuration management is contractually controlled by product design and management documentation, and imposes a management process for changes from qualified baseline designs.

- Customer requirements. Many A&D customers have formally recognized the reliability impact of Pb-free related changes, their potential impact on product performance and function. A change in function requires the change to be classified as major, requiring customer approval, and is thus the primary method of supplier control. Within this scope, individual programs may choose to control their own changes. Some programs and customers control Pb-free issues by requiring suppliers to prepare LFCP verified as compliant to GEIA-STD-0005-1. Few A&D customer requirements adequately address the changes involving Pb-free materials. Additionally, the requirements have not been coordinated among customers. DoD programs typically manage Pb-free issues through Parts, Materials, and Process (PMP) requirements, and some have begun to use new standards such as MIL-STD-3018 [2], for parts management, and GEIA-STD-0005-1 for LFCP.
- Standards and command media. Applicable standards include ANSI/EIA-649 [3], GEIA-STD-0005-1 (LFCP), and J-STD-609 [4].
- Program requirements and command media. Currently, the A&D industries lack a set of consistent program requirements and applicable command media to implement LFCP or other potential Pb-free solutions. Some organizations, such as the Pb-free Electronics Risk Management (PERM) consortium, sponsored by the Aerospace Industries Association (AIA), are promoting such consistent requirements, but have so far had limited success.

## 5. Sustainment

---

- Change control. Form, fit, and function considerations for Pb-free materials, e.g., part finishes and assembly solder, and processes changes, are not consistently interpreted. LFCPs address these concerns, but are not sufficiently implemented in the supply chain.
- COTS assembly management. EIA-933 [5] contains requirements to manage COTS assemblies, but for most COTS assemblies, the available COTS construction information is insufficient to assure Pb-free product performance or reliability.
- Spares provisioning. Current spares procurement requirements and processes do not address all Pb-free related system requirements.
- Solder alloy control. Solderability and storage conditions for Pb-free solder are currently not controlled adequately in most A&D repair activities.

### Issues/Gaps/Misconceptions

- Form, fit, and function. The interpretation of Pb-free changes on form, fit, and function for Pb-free materials are not consistent across A&D programs.
- COTS CM issues.
  - COTS assembly changes. Typically, COTS assemblies are purchased with little or no knowledge of the internal construction parts, materials, or processes. The introduction of Pb-free electronics will exacerbate this situation.
  - COTS assembly configuration control. The lack of configuration information for COTS items poses a risk that Pb-free materials and processes will be implemented in ways that do not meet system requirements.
- Spares contracts. Spares contracts and specifications may not capture all system requirements related to Pb-free electronics.
- Configuration control processes. Current A&D CM practices may not completely control assembly alloys, part finishes, and part temperature and moisture exposure to assure process compatibility and application performance.
- Configuration control requirements A&D CM requirements may not provide sufficient detail to assure that items meet system requirements with Pb-free related changes.



### Conclusions

Present practices include the essential elements for configuration management, but their current content is not adequate to address Pb-free related issues such as materials properties and compatibility. Updating will require a major effort by OEM's, contract manufacturers, material and parts suppliers, and DoD stakeholders to ensure proper configuration control and traceability to changes in designs, material compositions, and part replacements. There needs to be a sustainable effort to ensure that data and information regarding any constituent that goes into the construction of the electronic assemblies is known, documented, and properly communicated through the product life cycle.

### Recommendations

- Verification and qualification. Develop verification and qualification methods for Pb-free related changes for use as customer requirements. The methods should include periodic re-assessments to detect unanticipated effects of Pb-free materials and related changes to manage reliability risk. Define item requirements that meet system requirements to evaluate material set changes.
- Spares contracts. Develop spares contract requirements to assure meeting system requirements for Pb-free materials use and related changes.
- Requirements coordination. Develop methods to provide consistent Pb-free requirements. This involves formulating a set of metrics that will be agreed upon by both customer and supplier, that will define what the requirements are for Pb-free changes.
- Pure tin finish and solder alloy requirements. Develop requirements for introduction of pure tin finishes and Pb-free solders to be considered Class I (major) changes, unless it occurs within the framework of an approved LFCEP. All other changes are subject to a comprehensive review of all program issues.
- In-service data feedback. Update the in-service data feedback processes to detect Pb-free related problems. As appropriate, institute additional periodic inspections to provide additional insight into any systematic problems that have been incurred by the use of Pb-free. This information and data can be leveraged from stockpile testing and other related activities, as well as repair facility experience, to essentially promote an effort to gather and collect data for analysis, identification, and subsequent corrective actions that may need to be implemented.

## 5. Sustainment

- COTS periodic re-assessment. Develop performance verification processes for COTS assemblies to assess and report Pb-free related changes. Apply the processes periodically to confirm that performance is maintained.
- Customer verification of COTS configuration. Develop methods and requirements to document COTS assembly data when insufficient data is available from the manufacturer.
- COTS assembly repair. Develop processes to assure sufficient knowledge of parts and materials used in COTS assemblies to assure compatibility with repair materials and processes.
- Industry documents. Consolidate COTS assembly management requirements to address requirements of EIA-933, GEIA-STD-0005-1, and IEC TS 62239 [6].

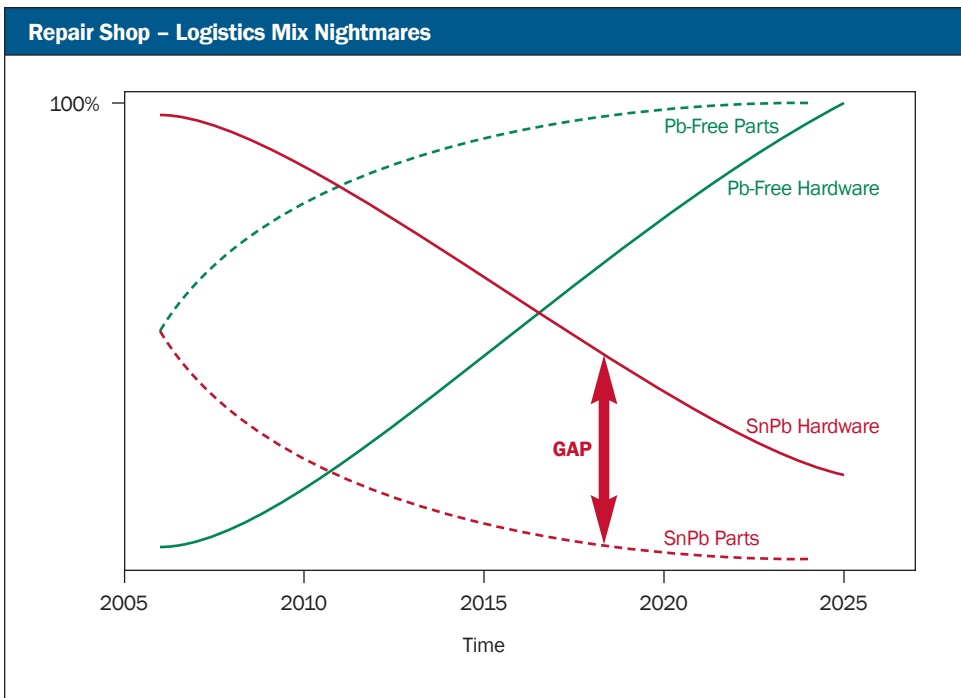
CM Concerns	Recommendations
Verification/Qualification	Develop methods for verification/qualification for use as customer requirements
Spares Requirements	Develop allocated and derived requirements for spares to assure that items meet system requirements
Requirements Coordination	Develop consistent customer requirements
Materials Changes	Develop requirements to assess pure tin introduction and solder alloy changes as major changes dependent on application
In-Service Feedback	Develop processes to identify Pb-free field issues
COTS Periodic Assessment	Develop performance verification processes to assess Pb-free impacts, and implement periodic assessment
COTS Configuration	Develop methods and requirements to document COTS materials as needed for system performance verification and sustainment
COTS Assembly Repair	Develop processes to assure compatibility of repair materials and processes with COTS configuration
Industry Documents	Consolidate COTS management requirements in various existing standards and update for Pb-free requirements

*Table 5.1 Configuration Management of Pb-Free Concerns. Specific CM practices will be impacted by introduction of Pb-free electronics.*

## 5.3 LOGISTICS

### Current Baseline Practices

- Customer requirements. Although current customer logistics requirements are based primarily on SnPb assemblies, some Pb-free requirements do exist. Again, a reiteration of the point must be made that although there is a mature infrastructure for logistics in general, the incorporation of Pb-free into the sustainment pipeline, which includes logistical support, is still in an embryonic stage.



**Figure 5.2 Logistics Management Challenges.** Increased mixing of assembly solder and part finishes will require practices to manage reliability impacts.

- Standards MIL-HDBK-502, Acquisition Logistics, airline practices, and document specific standard logistics practices. The general practices will not be affected by the introduction of Pb-free electronics, but there are issues with detailed implementation of specific elements.

## 5. Sustainment

---

### Issues/Gaps/Misconceptions

- Design interface. The Pb-free transition introduces the potential for new materials and processes to significantly affect logistics requirements, particularly repair practices, spares procurement, maintainability, and repairability. The interface between logistics disciplines and the design authority should address particular Pb-free issues.
- Level of repair. Level of repair analysis [7] will be impacted by the complexity of materials compatibility and degradation issues with Pb-free assemblies. These factors may contribute to a greater benefit in disposable electronics, instead of repairing electronics items that necessitate a higher level maintenance (e.g., require factory instead of field repair).
- Diagnostics and prognostics. The introduction of Pb-free assemblies will increase the potential for electrical shorts due to tin whiskers if not mitigated properly, and intermittent solder connections if the materials are not chosen properly. The diagnostic and prognostic practices will require adjustments to consider these effects.
- Spares provisioning. Spares requirements analysis will have to be updated to account for reliability and tin whisker impacts of Pb-free electronics.

### Conclusions

The Pb-free transition will have profound impacts on all elements of logistics management. Present practices include the essential elements for logistics management, but the materials properties and compatibility issues due to Pb-free electronics will require major changes in detailed implementation practices.

### Recommendations

- Implement LFCPs in accordance with GEIA-STD-0005-1 broadly across the A&D industry, supply chain, and logistics organizations.
- Identify customer requirements for logistics to manage the impacts of Pb-free parts, materials, and processes. These requirements should address factors such as standardization of solder alloys, materials identification, marking conventions, and process limitations.
- Develop and implement qualification procedures for repair and rework practices to assure maintenance of required reliability. These procedures need to address degradation of assemblies before introduction into the repair process.

- Develop metrics for level of repair analysis to address the challenges in repairing Pb-free assemblies. These considerations include materials compatibility, reliability degradation from storage, use, repair stresses, and part/component limitations on repair/rework cycles.
- Consider consolidation of commercial and military supply chain, e.g., Versa Module Eurocard suppliers could serve as contract manufacturers. Also, VME and similar circuit card assembly suppliers should become more active in the industry Pb-free activities.
- Implement Pb-free Control Plans in spares contracts to address criticality of part finishes and assembly solder alloys, to accommodate mixed material sets.
- Update diagnostic and prognostic processes to address Pb-free related failure modes, such as tin whisker shorts and solder joint opens, including intermittent failures.
- Implement programs to assess fielded Pb-free hardware degradation.

### 5.4 REPAIR

#### Current Baseline Practices

The current baseline practices for repair of CCAs and other assemblies are based on the assumption that SnPb is used for CCA assembly, and that SnPb-compatible coatings are used for printed wiring board bond-pad coatings, and finish coatings on the terminations of the piece parts. This assumption is so widespread that not all program requirements include the use of SnPb even though it is assumed. Very few A&D customer requirements have been updated to include Pb-free electronics.

Since the advent of Pb-free electronics, some additional resources have become available for A&D repair facilities to aid in addressing Pb-free issues. They are included in this description of current baseline practices, although they are not yet widely used or required on A&D programs. Most A&D repair processes are “OEM-unique,” and there are also considerable differences between the commercial and military segments of A&D. The DoD Lead Standardization Activity for Soldering Technology is working to provide common approaches across the DoD, and the Pb-free Electronics Risk Management Consortium is working to promote consistency across the A&D industries.

The elements of the repair process include (1) documentation, (2) materials, (3) equipment, (4) operator training, (5) repair procedures, and (6) shipping and handling procedures. All of these elements are discussed throughout the remainder of this section.

**Logistics Management**

Life Cycle Application

Maintenance Planning

Repair Analysis

Support and Test Equipment

Supply Support

Manpower, Personnel and Training

Facilities

Packaging, Handling, Storage  
and Transportation

Post Production Support

**Pb-Free Impacts**

Customer requirements to assure  
consideration of issues

Discard versus repair trade-offs

Spares provisioning due to reliability/  
repairability impact

Spares contracts to address  
performance and repair compatibility

Diagnostics for tin whiskers,  
intermittents

Procedures documentation

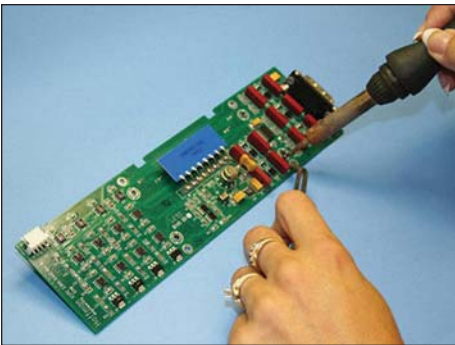
Repair processes qualification

Packaging and storage considerations  
for materials issues

Handling considerations for brittle  
intermetallics

Training for repair processes, handling

Equipment to manage Pb-free  
(e.g., XRF)



*Figure 5.3 Logistics Impact. Logistics management practices need to address Pb-free issues to avoid reliability degradation and support cost increases.*

*Documentation*

The basic process documents for repair of A&D assemblies are J-STD-001 [8] and IPC-7711/7721 [9]; they are used across programs and repair facilities. Repair facilities also may be guided for marking by J-STD-609. In addition, A&D organizations and repair facilities have their own documented repair processes. Many of those documents have been updated for Pb-free solder, but they contain very little hard data, and have not been verified for A&D applications.

Pb-free related issues that are likely to impact or be impacted by the repair process include:

- Solderability: Pb-free surfaces will be different and will be affected differently over time in typical storage conditions.
- Fluxes: used to repair Pb-free assemblies which may impact the reliability of the finished product.
- Cleaning materials and processes: used to repair Pb-free assemblies which may impact the reliability of the finished product.

It also must be noted that the repair requirements for a given assembly are produced and controlled by the design authority for that assembly, which is rarely the repair facility.

Pb-free specific repair documents include GEIA-STD-0005-1, GEIA-STD-0005-2 [10], GEIA-HB-0005-3 [11], and ARINC 671 [12]

### *Materials*

Current materials are based on SnPb solder. Some facilities are introducing Pb-free solder alloys, compatible fluxes and cleaning materials.

### *Equipment*

The basic equipment used for repair of A&D assemblies is based on SnPb solder. Some facilities have begun to update their equipment for Pb-free – and aside from the higher temperature requirements of some elements such as solder tips – few changes are expected.

### *Operator Training*

Current operator training is based on SnPb solder. The DoD Soldering Technology Working Group is developing training for DoD repair facilities, while some equipment manufacturers are developing their own training.

### *Repair Procedures*

Current repair procedures are based on SnPb solder. Some facilities are updating their procedures to address Pb-free. There are likely to be significant changes dictated by Pb-free solder.

### *Shipping and Handling Procedures*

Current shipping and handling procedures are based on SnPb solder. Some facilities have begun to update their procedures for Pb-free; but few changes are expected.

## 5. Sustainment

---

### Issues/Gaps/Misconceptions

The most serious issue related to the impact of Pb-free electronics on the repair process is the prospect of multiple manufacturers using an array of different solder alloys, all of which must be accommodated by the repair shop. This adds complexity to every repair activity, and increases the risks of reduced product reliability and loss of configuration control.

#### *Documentation*

The set of documents that currently exists for repair of A&D CCAs and other assemblies appears to be capable of accommodating the transition to Pb-free electronics. However, there is a need to review, revise and update all the existing documents as necessary to address specific issues related to Pb-free electronics.

It also must be noted that the industry documents prepared specifically for Pb-free electronics, e.g., references [7-9], are based on existing knowledge, and are thus provisional. They will have to be updated regularly as new knowledge, data, and experience become available.

Pb-free related issues that are likely to impact, or be impacted by the repair process include:

- Solderability: Pb-free surfaces will be different, and will be affected differently over time in typical storage conditions.
- Fluxes: used to repair Pb-free assemblies may impact the reliability of the finished product.
- Cleaning materials and processes: used to repair Pb-free assemblies may impact the reliability of the finished product.

These issues are not currently addressed in repair documentation. GEIA-STD-0005-1 describes the elements of a LFCP, and many A&D customers are requiring their suppliers to have LFCPs compliant to GEIA-STD-0005-1. It would be extremely beneficial to A&D repair facilities and their customers for the repair facility have an LFCP.

#### *Materials*

Repair shops are capable of effecting repairs on almost any given solder alloy, provided they are notified of the requirements for that alloy. (It is noted that it might not be necessary to use the exact same alloy for repair that was used for production; only that the repair alloy and associated processes are capable of restoring the assembly to its original state.) The significant risk, as stated above, is that a multitude of alloys will be used in the various production facilities, and that all of them will have to be accommodated in the repair facility.



\*Note: It is tempting to consider some high-level restrictions on the number of assembly alloys that would be allowed by the A&D industries, and some form of such restriction may be necessary. If this course is taken, it would have significant impacts in other parts of the industries, and many other factors besides design, production, and repair must be considered.

### *Equipment*

There is few equipment issues associated with Pb-free electronics that cannot be addressed with the existing resources. A prime example of this would be a change in the material construction of a solder pot holding Pb-free solders.

### *Operator Training*

All repair facility operators will have to be trained in the use of Pb-free solder. The training should include necessary techniques, inspection methods, storage, and handling. An important Pb-free impact will be in troubleshooting failures to identify those related to Pb-free electronics. Training methods will have to be developed. This is a significant gap.

### *Repair Procedures*

Repair documentation will have to be updated to accommodate Pb-free electronics, such as inclusion of enhanced bake-out processes prior to reflowing solder to protect moisture and temperature sensitive parts and PCBs. Procedures will need to apply adequate controls to address the impacts of material and tool cross-contamination.

### *Shipping and Handling Procedures*

Repair documentation will have to be updated to accommodate Pb-free electronics.

## **Conclusions**

### *Documentation*

The basic process document for repair of A&D assemblies is IPC-7721, which is used across programs and repair facilities. Repair facilities also may be guided by J-STD-001. In addition, A&D organizations and repair facilities have their own documented repair processes. Many of those documents have been updated for Pb-free solder, but they contain very little hard data, and have not been verified for A&D applications. It also must be noted that the repair requirements for a given assembly are produced and controlled by the design authority for that assembly, which is rarely the repair facility. Pb-free specific repair documents include GEIA-STD-0005-1, GEIA-STD-0005-2, GEIA-HB-0005-3, and ARINC 671.

## 5. Sustainment

---

### *Materials*

Current materials are based on SnPb solder. Some facilities are introducing Pb-free solder alloys, and compatible fluxes and cleaning materials.

### *Equipment*

The basic equipment used for repair of A&D assemblies is based on SnPb solder. Some facilities have begun to update their equipment for Pb-free, and aside from the higher temperature requirements of some elements such as solder tips and rework stations, few changes are expected.

### *Operator Training*

Current operator training is based on SnPb solder. The DoD Soldering Technology Working Group is developing training for DoD repair facilities, while some equipment manufacturers are developing their own training. Operators may have to be re-certified in certain aspects of repair, for example, in areas of high reliability assemblies.

### *Repair Procedures*

Current repair procedures are based on SnPb solder. Some facilities are updating their procedures to address Pb-free. There are likely to be significant changes dictated by Pb-free solder.

### *Shipping and Handling Procedures*

Current shipping and handling procedures are based on SnPb solder. Some facilities have begun to update their procedures for Pb-free, but few changes are expected.

## **Recommendations**

### *Documentation*

Review all A&D repair facility documentation for Pb-free impact and revise if necessary.

Based on the above review, provide information related to the impact of the design on repairability and the repair process, to the design authorities and manufacturing organizations for all hardware that will be repaired in the given repair facility.

Of particular concern is the impact of multiple solder alloys used in the original assemblies, all coming from various assembly facilities, which may require a given repair facility to maintain an unacceptably wide range of solder alloys to be used for repair. Solutions to be considered are:

- Restrict the number of assembly solder alloys specified by the design authority to SnPb and a small number of Pb-free alloys that are compatible with one or two Pb-free repair alloys.

- Review all industry documents related to Pb-free repair, e.g., references [7-9], to ensure that they are up to date, and revise as necessary to incorporate recent knowledge, experience, and data.

Update repair documentation to address Pb-free related issues that are likely to impact, or be impacted by, the repair process including:

- Solderability: Pb-free surfaces will be different, and will be affected differently over time in typical storage conditions.
- Fluxes: used to repair Pb-free assemblies may impact the reliability of the finished product.
- Cleaning materials and processes: used to repair Pb-free assemblies may impact the reliability of the finished product.

Require A&D repair facilities to have Pb-free Control Plans Compliant to GEIA-STD-0005-1.

### *Materials*

Coordinate among A&D repair facilities and design authorities to ensure visibility into the assembly alloys used in original assemblies, and to develop and maintain repair alloys that are compatible with the original assembly alloys. Update repair procedures to include methods to assure material and process compatibilities of the finishes, solders, and fluxes that meet reliability requirements.

### *Equipment*

Coordinate among A&D repair facilities and design authorities to ensure visibility into the assembly alloys used in original assemblies, and to develop and maintain repair equipment that is compatible with the original assembly alloys.

### *Operator Training*

Update A&D repair facility training programs to ensure repair capabilities with all relevant Pb-free solder alloys. Of particular concern are the inspection procedures for incoming product to identify assembly alloys and outgoing product in order to ensure reliability.

### *Repair Procedures*

Update A&D repair facility repair procedures to ensure repair capabilities with all relevant Pb-free solder alloys. The procedures should be assessed by the IPC Pb-free process certification. Inspection processes for tin whiskers must be included in repair procedures.

### *Shipping and Handling Procedures*

Update A&D repair facility shipping and handling procedures to ensure repair capabilities with all relevant Pb-free solder alloys.

## 5. Sustainment

Repair Elements	Baseline Practices	Recommendations
Documentation	J-STD-001, IPC-7711/7721, IPC-A-610, J-STD-609, Technical Manuals and similar repair procedures	<ul style="list-style-type: none"><li>• Restrict designed solders and finishes to be compatible with a limited set of repair solder alloys</li><li>• Keep industry standards current</li><li>• Update repair processes to address factors such as solderability, flux use, and cleaning</li><li>• Implement Pb-free Control Plans at repair activities</li></ul>
Materials	Based on SnPb solder, with some updates for Pb-free materials	<ul style="list-style-type: none"><li>• Coordinate between repair facilities and design activity for optimum material set selection</li><li>• Assure compatibility of finishes, solders, fluxes in repair process to assure reliability</li></ul>
Equipment	Based on SnPb solder, some inherent Pb-free capability	<ul style="list-style-type: none"><li>• Assure compatibility of repair equipment with designed hardware and repair processes</li></ul>
Operator Training	Based on SnPb solder, and some early efforts to address Pb-free materials	<ul style="list-style-type: none"><li>• Update training programs for Pb-free processes</li><li>• Address inspection of incoming hardware to identify finishes and solders that affect repair</li><li>• Address inspection of ongoing hardware for reliability</li></ul>
Repair Procedures	Based on SnPb solder with some updates to address Pb-free solder and finishes	<ul style="list-style-type: none"><li>• Update repair procedures to assure capability with all applicable finishes and solders</li><li>• Utilize IPC Pb-free process certification process</li><li>• Implement tin whisker inspection approaches</li></ul>
Shipping and Handling (S&H) Procedures	Based on SnPb solder	<ul style="list-style-type: none"><li>• Update S&amp;H procedures to assure capability with Pb-free finishes and solders</li></ul>

Table 5.2 Impact on Repair: Repair practices require updates to address use of Pb-free finishes and solders.

“Those are my principles, and if you don’t like them ... well, I have others.”

*—Groucho Marx (1890-1977)*



# 6. Testing

## 6.1 INTRODUCTION

Current test methodologies are not adequate for qualification and acceptance of Pb-free aerospace and defense electronics. Design and production engineers rely on these tests to develop and deliver reliable electronics for the warfighter. As a consequence, the reliability of Pb-free electronics cannot currently be guaranteed to meet the reliability of A&D programs.

The greatest reliability risks associated with Pb-free electronics are the formation of tin whiskers, solder joint failures due to vibration and mechanical shocks, and the lack of validated models required to design tests and predict field lifetimes of electronics. Such models exist for SnPb only.

The formation of tin whiskers threatens the reliability of A&D systems that use Pb-free surface finishes and solders. Current tin whisker testing methods cannot predict whether a finish or solder will grow tin whiskers (Table 6, Specification and Standard Table, located in Appendix A). In addition, existing whisker mitigation strategies are only partially effective (GEIA-STD-0005-2). Reliable whisker test methods and mitigation strategies need to be developed based upon a fundamental knowledge of whisker growth mechanisms.

The testing gap associated with Pb-free will not necessarily require new equipment capabilities, but will require redefining the test parameters under which the equipment will perform. ESS, verification, validation, acceptance, and qualification tests for Pb-free production hardware require that new test parameters (temperature extremes, dwell times, vibration environments, etc.) be defined. Validated computational models need to be developed to define these parameters, and to link them to actual field conditions and service lifetimes. These models currently do not exist or are in the very embryonic stages, and have not been adequately validated. Furthermore, the fidelity of computational modeling predictions depends upon the development of accurate mechanical and physical property data for Pb-free solders, PWB laminates and component package materials. Standardized materials testing needs to be done to provide the basic material properties required for input into and validation of the computational models for Pb-free electronics.

Other Pb-free reliability issues that have been identified include PCB delamination, PTH reliability, copper dissolution, CAF formation, pad cratering, trace cracking, corrosion, and voiding problems associated with PCB finishes during the high temperature Pb-free processing. Industry standards, while available for SnPb electronics, need to be created or modified to specifically address these issues for Pb-free electronics.

## **6.2 TESTING FOR MATERIALS PROPERTIES AND PRODUCT MANUFACTURABILITY**

### **FOR Pb-FREE CIRCUIT CARD ASSEMBLIES**

#### **Current Baseline Practice**

The materials test methods, acceptance, and qualification standards required for evaluating materials for Pb-free assembly, including laminates, copper, components, solder paste, and fabricated PCBs, are generally the same for consumer, commercial, and A&D applications. As a result of this shared standards base, the microelectronics industry has modified, or is in the process of modifying, all the requisite standards for assessing Pb-free CCAs. The flow of test method, verification, acceptance, and qualification standards from the individual materials, through acceptance of the CCA, is shown in Figure 6.1.

All of the standards in Figure 6.1 are dependent standards required by IPC/EIA J-STD-001 "Requirements for Soldered Electrical and Electronic Assemblies" which describes materials, methods, and verification criteria for producing soldered interconnections on CCAs. All of these underlying standards are supported by numerous additional standard test methods, many of which are in the IPC-TM-650. With the exception of tin whisker testing standards and more explicit test parameters needed for consistent Pb-free testing, the impact of the transition to Pb-free CCAs will be minimal due to the additional changes in these standards, since many have been created or modified for Pb-free. The greater impact for A&D products is in the extensive verification, validation, acceptance, and qualification testing that will be required for manufacturing Pb-free CCAs. A list of materials properties most affected by the Pb-free transition and their underlying standards is provided in Table 6, located in the appendix.

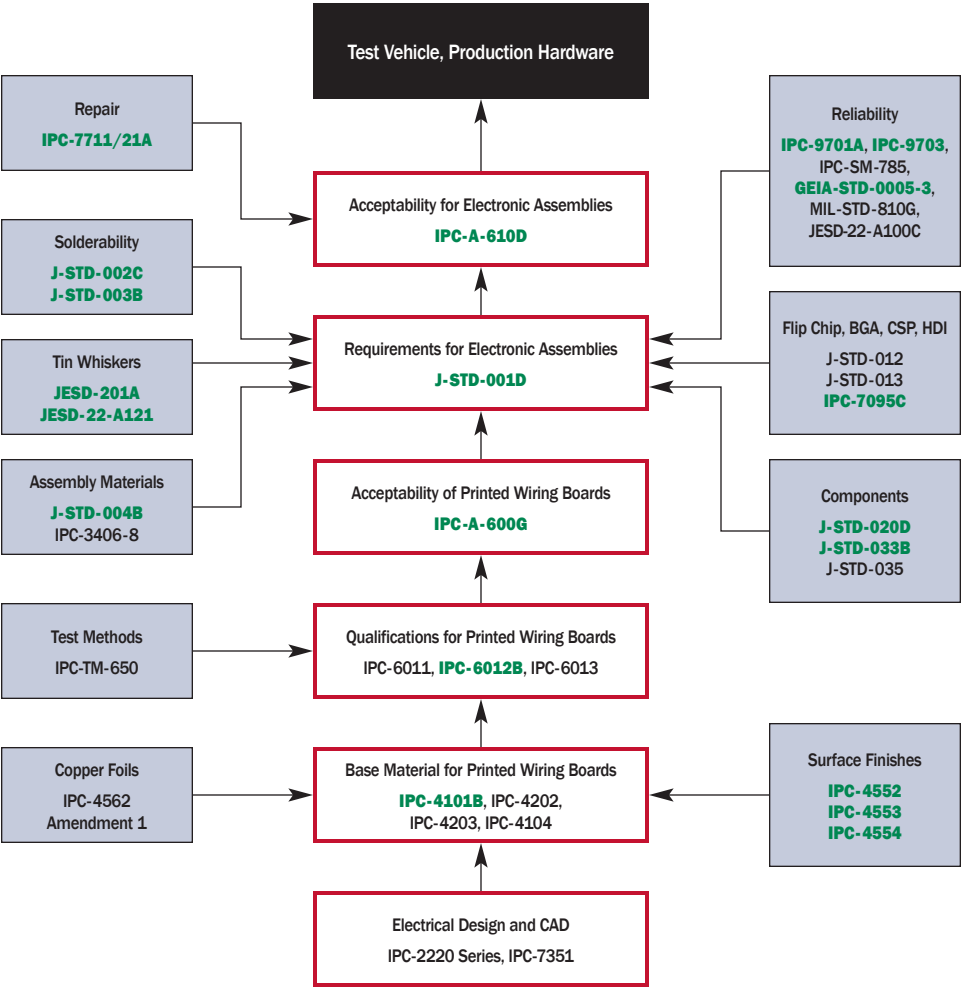


Figure 6.1 IPC Standards Chart

6.2.1 PCB Materials and Manufacturing for Pb-free CCAs

The individual materials for fabricating PCBs, including laminate, surface finishes, and copper are evaluated according to specifications shown in the proceeding tables. Of the many properties called out in these test method standards, Pb-free manufacturing for A&D will have the greatest impact on the following properties.



- Solderability for PCBs  
The standard specifies using SAC305 solder and paste. “Other Pb-free solder alloys may be used upon agreement between user and vendor.”

Baseline Practice	Test and Applicable Standard	Is the Current Test Equipment Adequate for Pb-Free?	Are the Current Test Parameters Adequate for Pb-Free?
Solderability (Dip and Look, Wave Solder)	IPC J-STD-003B “Solderability for Printed Boards,” March 2007	Yes	Yes

Table 6.1 Solderability for PCBs

- Electromigration  
This test method provides a means to assess the propensity for surface electrochemical migration. This test method can be used to assess soldering materials and processes.

Baseline Practice	Test and Applicable Standard	Is the Current Test Equipment Adequate for Pb-Free?	Are the Current Test Parameters Adequate for Pb-Free?
Electromigration Testing	IPC-TM-650, Method 2.6.14.1F, “Electrochemical Migration Resistance Test,” September 2000	Yes	Yes

Table 6.2 Electromigration Testing

- Tin Whisker Assessment of PCB  
There are no tin whisker test methods, acceptance or qualification standards, for board surface finishes for A&D electronics. The Class 1 and 2 acceptance standard JEDEC JESD201 is explicitly for components and connectors. Other sources of whisker threats come from the Pb-free surface finishes used on non-electronic hardware such as RF boxes (e.g., satellites, communication systems, RF links, radio applications), card rails (e.g., Space Shuttle *Endeavor*) and mechanical connectors (tin or zinc plated hardware such as screws, washers, etc).

IPC-4554 states “...the test method will be used with the understanding that the responsibility to verify the impact of potential whisker growth on a module’s long term reliability is the end users. See Appendix 6 for JEDEC/IPC PCB paragraphs.”

6. Testing

Baseline Practice	Test and Applicable Standard	Is the Current Test Equipment Adequate for Pb-Free?	Are the Current Test Parameters Adequate for Pb-Free?
PCB Tin Whiskers	No Industry Standard Test Method Exists	No	No

Table 6.3 Tin Whisker Assessments

- Surface Finish Verification (XRF)  
This current specification is in the drafting stage.

Baseline Practice	Test and Applicable Standard	Is the Current Test Equipment Adequate for Pb-Free?	Are the Current Test Parameters Adequate for Pb-Free?
Surface Finish Verification (XRF)	MIL-STD-1580 (Draft), “Detailed Requirements for Prohibited Materials Analysis and Incoming Inspection of External Package Plating Materials Using X-Ray Fluorescence Spectroscopy or Scanning Electron Microscopy with Energy Dispersive Spectroscopy”	Yes (Draft)	Yes (Draft)

Table 6.4 Surface Finish Verification

- PCB Delamination  
Method 2.4.24.1 describes the method for determining the time to delamination of laminates and PCBs through the use of a thermo-mechanical analyzer (TMA).

This test method 2.4.13.1 is designed to determine the thermal integrity of unclad or metallic clad laminates using short-term solder exposure.

Test method 2.4.23 specifies SnPb in test. This test method is used to determine the resistance of laminate materials (both unclad and etched surfaces) to the thermal abuse of a solder dip.

Baseline Practice	Test and Applicable Standard	Is the Current Test Equipment Adequate for Pb-Free?	Are the Current Test Parameters Adequate for Pb-Free?
PCB Delamination Test	IPC-TM-650, Method 2.4.24.1, "Time to Delamination," December 1994	Yes	With Modifications
	IPC-TM-650, Method 2.4.13.1, "Thermal Stress of Laminates," December 1994	Yes	With Modifications
	IPC-TM-650, Method 2.4.23, "Soldering Resistance of Laminate Materials," March 1979	Yes	With Modifications

Table 6.5 PCB Delamination

- PCB CAF Testing  
This method does not discuss exposure to thermal environments before testing. The higher temperatures associated with the insertion of Pb-free processes, along with the higher and lower environmental temperatures which will be required for a proper assessment of Pb-free reliability, may make some pre-testing conditions necessary for this test.

Baseline Practice	Test and Applicable Standard	Is the Current Test Equipment Adequate for Pb-Free?	Are the Current Test Parameters Adequate for Pb-Free?
PCB Conductive Anodic Filament (CAF)	IPC-TM-650, Method 2.6.25, "Conductive Anodic Filament Resistance Test: X-Y Axis," November 2003	Yes	With Modifications

Table 6.6 PCB CAF Testing

- PCB IST (Interconnect Stress Testing)  
Currently used for Pb-free per specifications in IPC-6012 for bare PCBs.

6. Testing

Baseline Practice	Test and Applicable Standard	Is the Current Test Equipment Adequate for Pb-Free?	Are the Current Test Parameters Adequate for Pb-Free?
PCB Interconnect Stress Testing (IST)	PC-TM-650, Method 2.6.26, "DC Current Induced Thermal Cycling Test," November 1999	Yes	Yes

Table 6.7 PCB Interconnect Stress Testing

- Copper Testing
  - Copper Dissolution Test  
An industry practice exists for this test, but falls short when applied to Pb-free because the problem is exacerbated due to the increased temperature conditions.
  - Copper Strength and Elongation for Electrodeposited Copper  
This test determines the tensile strength in MPa (psi) and the elongation, in percentage, of electrodeposited copper plating at ambient temperatures by mechanical force testing.
  - Copper Strength and Elongation, Copper Foil  
This test determines the tensile strength in MPa (psi) and the elongation (in percentage) of copper foil at ambient and elevated temperatures by mechanical force testing.

Baseline Practice	Test and Applicable Standard	Is the Current Test Equipment Adequate for Pb-Free?	Are the Current Test Parameters Adequate for Pb-Free?
Cu Dissolution Test	No Industry Standard Test Method Exists	No	No
PCB Copper Test, Electrodeposited Copper	IPC-2.4.18.1, "Tensile Strength and Elongation, In-House Plating," May 2004	Yes	Yes
PCB Copper Test, Copper Foil	IPC-2.4.18, "Tensile Strength and Elongation, Copper Foil," August 1980	Yes	Yes

Table 6.8 Copper Testing

6.2.2 Component Testing for Pb-Free CCAs

Components are evaluated according to specifications shown in the proceeding tables. Of the many requirements called out in these test methods which specify particular property attributes pertaining to the performance of components, the effect of inserting Pb-free into the manufacturing stream will impact the results, and subsequently the test method for A&D applications.

- Surface Finish Verification (XRF), Component Solderability  
This current specification for XRF is presently in the drafting stage.

The standard for component solderability describes test methods, defect definitions, acceptance criteria, and illustrations for assessing the solderability of electronic component leads, terminations, solid wires, stranded wires, lugs, and tabs. This standard also includes a test method for the Resistance to Dissolution/Dewetting of Metallization. This standard is intended for use by both vendor and user.

Baseline Practice	Test and Applicable Standard	Is the Current Test Equipment Adequate for Pb-Free?	Are the Current Test Parameters Adequate for Pb-Free?
Surface Finish Verification (XRF)	MIL-STD-1580 (Draft), "Detailed Requirements for Prohibited Materials Analysis and Incoming Inspection of External Package Plating Materials Using X-Ray Fluorescence Spectroscopy or Scanning Electron Microscopy with Energy Dispersive Spectroscopy"	Yes (Draft)	Yes (Draft)
Component Solderability	IPC/EAC J-STD-002C, "Solderability Tests for Component Leads, Terminations, Lugs, Terminals and Wires," November 2008	Yes	Yes

Table 6.9 Component Testing for Pb

6. Testing

- **Component Tin Whisker Assessment**  
Tin whisker test methods, acceptance and qualification standards for components do not exist for Class 3 A&D electronics. The JEDEC standard JESD22-A121A “Test Method for Measuring Whisker Growth on Tin and Tin Alloy Surface Finishes” is not a qualification standard. Its purpose is only to recommend whisker growth test conditions so that data collected industry-wide can be compared and used to improve the understanding of whisker growth. The environmental (temperature/humidity) acceptance requirements in the JEDEC standard JESD201 for Pb-free components are a minimum six-month testing period for two of the three required tests and retesting of components for almost every change in component, surface finish, or plating conditions. JESD201 states that this standard “does not apply to components with bottom-only terminations where the full plated surface is wetted during assembly (for example: QFN and BGA components, flip chip bump terminations).” Both JESD22-A121A and JESD201 are for consumer electronics only, and explicitly state they are not sufficient for A&D applications. The JESD22-A121A test method may not be sufficient for applications with special requirements, e.g., military or aerospace, while the JESD201 does not address the uncertainty of the tin whisker growth incubation period (hours to years) which confounds the qualification tests for surface finishes on printed circuit boards, components, and circuit card assemblies.

Baseline Practice	Test and Applicable Standard	Is the Current Test Equipment Adequate for Pb-Free?	Are the Current Test Parameters Adequate for Pb-Free?
Component Tin Whisker Assessment	JESD-22-A121A, “Test Method for Measuring Whisker Growth on Tin and Tin Alloy Surface Finishes,” July 2008	No	No
	JESD-201, “Environmental Acceptance Requirements for Tin Whisker Susceptibility of Tin and Tin Alloy Surface Finishes,” September 2008	No	No

Table 6.10 Component Tin Whisker Assessment

### 6.2.3 Solder Testing

Solder alloy, paste, and flux testing for assembling Pb-free CCAs was one of the first areas addressed in the consumer electronics transition to Pb-free. Solders are evaluated according to specifications shown in the proceeding tables. Of the many properties called out in these test method standards, Pb-free manufacturing for A&D will have the greatest impact on the properties that follow.

- **Paste Solderability Testing**  
One test method (2.4.46) specifies using Sn60 solder, while the other (2.4.45) method does not mention the solder type.

Baseline Practice	Test and Applicable Standard	Is the Current Test Equipment Adequate for Pb-Free?	Are the Current Test Parameters Adequate for Pb-Free?
Paste Solderability Testing	IPC-TM-650, Method 2.4.46 Rev. A, "Spread Test, Liquid, Paste or Solid Flux, or Flux Extracted from Solder Paste, Cored Wires or Performs," June 2004	Yes	With Modifications
	IPC-TM-650, Method 2.4.45, "Solder Paste – Wetting Test," January 1995	Yes	With Modifications

**Table 6.11 Solder Testing**

- **Surface Insulation Resistance (SIR) Testing**

Baseline Practice	Test and Applicable Standard	Is the Current Test Equipment Adequate for Pb-Free?	Are the Current Test Parameters Adequate for Pb-Free?
Surface Insulation Resistance (SIR)	IPC-TM-650, Method 2.6.3.3 Rev. B, "Surface Insulation Resistance, Fluxes," June 2004	Yes	Yes

**Table 6.12 SIR Testing**

6. Testing

- **Tin Pest Testing**  
In addition to forming tin whiskers, tin can sometimes undergo a phase transformation from beta-tin (body centered tetragonal) into alpha-tin (diamond cubic) at temperatures below 13 °C. This transformation is called “tin pest.” The change is accompanied by an increase in volume of 26 percent which results in disintegration of the tin. The maximum rate of the phase transformation appears to occur between -30 and -35 °C. Current industry practice for SnPb is currently comprised of a test which maintains an isothermal hold of -40 °C, until the tin pest appears. No test standard currently exists for assessing tin pest formation in Pb-free electronics. See Section 7.0, Reliability for more information.

Baseline Practice	Test and Applicable Standard	Is the Current Test Equipment Adequate for Pb-Free?	Are the Current Test Parameters Adequate for Pb-Free?
Tin Pest	No Industry Standard Test Method Exists	No	No

Table 6.13 Tin Pest Testing

- **Solder Joint Tin Whisker Assessment**  
There are no tin whisker test methods, acceptance, or qualification standards for solder alloys and solder pastes for A&D electronics. The tendency to form whiskers on Pb-free solder joints has been found to be increased by residual surface contamination after reflow, thermal expansion differences between the solder and the component lead material, alloy doping elements, particular rare earth additions, reflow atmosphere, and corrosion. Test method, acceptance, and qualification standards for Pb-free solder joints are needed for solder and paste developers and design engineers to quantify the propensity of solder alloys and pastes to form whiskers.

Baseline Practice	Test and Applicable Standard	Is the Current Test Equipment Adequate for Pb-Free?	Are the Current Test Parameters Adequate for Pb-Free?
Solder Joint Tin Whisker Assessment	No Industry Standard Test Method Exists	No	No

Table 6.14 Solder Joint Tin Whisker Assessment



---

---

### Issues/Gaps/Misconceptions

- Issue: It is currently not possible to predict whisker formation and growth. Tin whisker qualification tests for surface finishes are confounded by the uncertainty of the tin whisker growth incubation period (hours to years). System reliability can be threatened by the use of Pb-free surface finishes on non-electronic hardware such as RF boxes (satellites), card rails (e.g., Space Shuttle *Endeavor*) and mechanical connectors (screws, washers, etc.).
- Issue: Current specifications for PCBs do not provide sufficient guidance in terms of test parameters. For example, current baseline practice for testing Pb-free PCBs requires testing of both as-fabricated boards and boards exposed to five times simulated reflow at 260°C. The five temperature exposures were recommended by the International Electronics Manufacturing Initiative (iNEMI) based on topside reflow, bottom side reflow, one wave soldering pass, one exposure each for rework, and attaching a missing part. However, these procedures are not explicitly stated in any standard. Current baseline practice for SnPb CCAs is testing as-fabricated boards and boards exposed to three times reflow at 240°C.
- Issue: The manufacturing process window is significantly smaller for Pb-free CCAs than SnPb CCAs. Materials suppliers and PCB manufacturers must retest and report more frequently on PCBs, components, and other materials that go into Pb-free CCAs to demonstrate manufacturing capability and quality control.
- Gap: Test methods, acceptance, and qualification standards for tin whiskers on components, board surface finishes, and solder joints do not exist for A&D electronics. More fundamental research is needed to understand the whisker growth mechanism and predictive models of whisker propensity need to be developed.
- Gap: Current specifications need to be modified for PCB delamination, CAF testing, and paste solderability. New specifications need to be developed for copper dissolution and tin pest.
- Gap: There are no predictive test methods for Pb-free interconnect failure modes such as pad lifting, pad cratering, interface delamination, and trace fracture. The current standards shown in Figure 6.1 and the preceding tables were established to eliminate other, more common failure modes. As additional failure modes and their root causes are identified, it is expected that test method standards, test conditions, acceptance standards and qualification standards for Pb-free assembly materials and PCB testing will change significantly. It is imperative that this relationship between significant failure modes and PCB properties be established, with a feedback loop into the standards, in order to improve the robustness and reliability of Pb-free assemblies and systems.

## 6. Testing

---

### Conclusions

Current tin whisker and PCB materials testing methods are inadequate for Pb-free A&D electronics.

The formation of tin whiskers poses a high reliability risk to systems using Pb-free surface finishes and solders, including those on non-electronic hardware such as RF boxes (satellites), card rails (e.g., Space Shuttle *Endeavor*) and mechanical connectors (screws, washers, etc.).

Reliability of Pb-free electronics could greatly improve from whisker mitigation strategies based on fundamental knowledge of the whisker growth mechanism. Tin whisker evaluation of printed circuit board surface finishes, such as immersion tin, hot air solder leveled (HASL) Pb-free alloys, and Pb-free solder alloys and pastes needs to be addressed for A&D electronics.

### Recommendations

Effective tin whisker mitigation methods need to be developed for Pb-free A&D electronics. Efforts to determine the fundamental mechanism for tin whisker growth should continue and acceleration factors for modeling need to be determined. Standard JEDEC JESD201 can serve as an interim strategy for A&D electronics until a predictive test has been accepted. Standard JEDEC JESD201 should not be used as an acceptance document for A&D electronics.

Current specifications need to be modified for PCB delamination, CAF testing, and paste solderability. New specifications need to be developed for copper dissolution and tin pest.

## 6.3 MATERIAL TESTING FOR COMPUTATIONAL MODELING

Computational modeling provides the means to predict the long-term fatigue performance of Pb-free solder interconnections in place of extensive laboratory test programs. Large-scale test programs are becoming cost prohibitive because of the growing range of materials sets, solder joint geometries and tests, as well as service environments. (See Section 7.0, Reliability, for a discussion on models.)

Modeling is used to determine hardware test parameters for verification, validation, acceptance, or qualification of Pb-free solder interconnections that are based upon actual service lifetimes rather than only “lower bounds” benchmarks, as provided by current specifications. This approach avoids under-testing the interconnections, resulting in a service reliability shortfall, or over-testing, which results in hardware over-design and excessive product scrap.

The fidelity of computational modeling predictions depends upon the accuracy of the mechanical and physical properties for the solder, as well as substrate laminate and component package materials (e.g., ceramic, plastic, etc.). Standardized material testing is required to provide accurate mechanical and physical materials properties as input data for the computational models.

Current Baseline Practice

Materials testing methods can provide early validation of the computational model predictions. Test data – stress-strain curves, strain-time curves (creep), and hysteresis loops (isothermal fatigue) – provide validation of the constitutive equation by comparing empirical and predicted curves versus temperature, strain rate, etc. In addition, the data obtained from the testing of simulated solder joints provides validation of the combined constitutive equation and finite element functions within the model.

6.3.1 Stabilization and Other Annealing Treatments

Mechanical and physical properties of metal alloys are sensitive to the *as-solidified* microstructure (grain size, dislocation density, etc.). Stabilizing the material microstructure prior to testing can reduce the variability of those measured properties. The stabilization treatment provided in IPC-9701A for SnPb and SnAgCu is 100 °C, 24 hours. This value is not based upon the rate kinetics of a microstructure process and may not be applicable to other Pb-free solders.

In many circumstances, solder joints are exposed to additional elevated temperature environments prior to, as well as during, service lifetimes. Isothermal annealing treatments are used to simulate such exposures so that their impact on the mechanical and physical properties can be documented.

It is necessary that metallographic cross sections be made before and after stabilization or other annealing treatment to document the resulting microstructure. Establishing stabilization treatments based upon microstructure kinetics for each alloy will be needed. Isothermal annealing treatments may also be required to simulate follow-on manufacturing and test conditions, as well as harsh service environments.

Baseline Practice	Test and Applicable Standard	Is the Current Test Equipment Adequate for Pb-Free?	Are the Current Test Parameters Adequate for Pb-Free?
Stabilization and Other Annealing Treatments	IPC-9701A, “Performance Test Methods and Qualification Requirements for Surface Mount Solder Attachments,” February 2006	Yes	With Modifications

Table 6.15 Stabilization Treatments

## 6. Testing

### 6.3.2 Time Independent Monotonic (Stress-Strain) Mechanical Properties

Time independent monotonic (stress-strain) mechanical properties are required of the Pb-free solder, printed circuit board, and component materials. Test temperatures and strain-rates must bound those values anticipated for the interconnections when exposed to service and all test conditions. The starting and ending microstructures should be documented by metallographic cross sections.

The required data are the strain-time curves, yield strength, ultimate strength, Poisson’s ratio, work hardening and work softening parameters, and static modulus. All solder compositions can be evaluated by the ASTM test methods listed in the proceeding tables. Modifications to the sample geometry and test fixture are required for test specimens having size scales equivalent to the microstructure.

The acoustic wave technique is an alternative method to obtain the elastic and shear moduli as well as Poisson’s ratio. These parameters are then referred to as dynamic properties. Some ASTM test methods do not address the microstructure size scale effect in the testing of solder alloys. The standard test specimen geometries are not adequate, and it is recommended that alternative, smaller sample geometries be considered. The list includes:

- ASTM E8/EM8 - 08
- ASTM E21 - 05
- ASTM E209 - 00 (2005)
- ASTM E111 - 04
- ASTM E143 - 02 (2008)
- ASTM E1876 - 07

Baseline Practice	Test and Applicable Standard	Is the Current Test Equipment Adequate for Pb-Free?	Are the Current Test Parameters Adequate for Pb-Free?
Time Independent Monotonic (Stress Strain) Mechanical Properties	ASTM E8/E8M - 08 Standard Test Methods for Tension Testing of Metallic Materials	Yes	With Modifications
	ASTM E21 - 05 Standard Test Methods for Elevated Temperature Tension Tests of Metallic Materials	Yes	With Modifications

Baseline Practice	Test and Applicable Standard	Is the Current Test Equipment Adequate for Pb-Free?	Are the Current Test Parameters Adequate for Pb-Free?
	ASTM E209 - 00 (2005) Standard Practice for Compression Tests of Metallic Materials at Elevated Temperatures with Conventional or Rapid Heating Rates and Strain Rates	Yes	With Modifications
	ASTM E111 - 04 Standard Test Method for Young's Modulus, Tangent Modulus, and Chord Modulus	Yes	With Modifications
	ASTM E143 - 02 (2008) Standard Test Method for Shear Modulus at Room Temperature	Yes	With Modifications
	ASTM E1876 - 07 Standard Test Method for Dynamic Young's Modulus, Shear Modulus, and Poisson's Ratio by Impulse Excitation of Vibration	Yes	With Modifications
	ASTM C1273 - 05 Standard Test Method for Tensile Strength of Monolithic Advanced Ceramics at Ambient Temperatures	Yes	Yes
	ASTM C1366 - 04 Standard Test Method for Tensile Strength of Monolithic Advanced Ceramics at Elevated Temperatures	Yes	Yes
	ASTM D638 - 08 Standard Test Method for Tensile Properties of Plastics	Yes	Yes

## 6. Testing

Baseline Practice	Test and Applicable Standard	Is the Current Test Equipment Adequate for Pb-Free?	Are the Current Test Parameters Adequate for Pb-Free?
	ASTM E345 - 93 (2008) Standard Test Methods of Tension Testing of Metallic Foil	Yes	Yes

Table 6.16 Time Independent Mechanical Testing

### 6.3.3 Time-Dependent Monotonic (Creep) Mechanical Properties

Time-dependent (creep) deformation properties are required of the solder, printed circuit board, and component materials. Test temperatures and applied stresses must bound the anticipated interconnection service and the test environments. The starting and ending microstructure should be documented by metallographic cross section techniques.

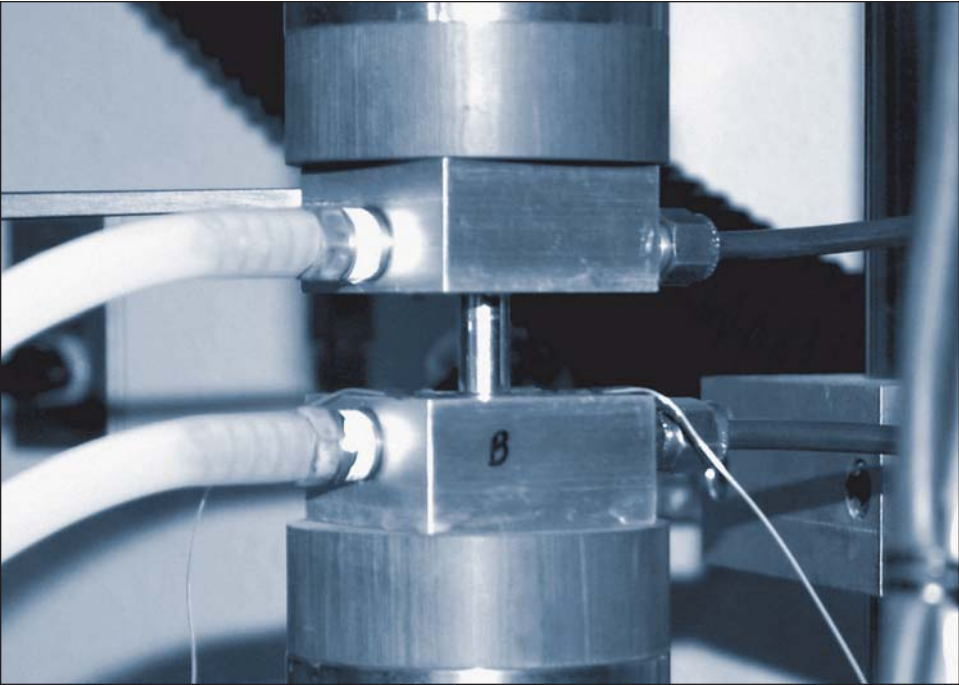


Figure 6.2 Compression Creep Testing

The required data consists of the strain-time curves and rate kinetics parameters of the steady-state creep stage, power law stress exponent (or  $\sinh$  term exponent), and the apparent activation energy. All solder compositions can be evaluated by the ASTM test methods listed in Table 6.17. As with the methods for determining the time independent creep properties, modifications to the sample geometry and test fixture are required for test specimens having size scales equivalent to the microstructure.

Baseline Practice	Test and Applicable Standard	Is the Current Test Equipment Adequate for Pb-Free?	Are the Current Test Parameters Adequate for Pb-Free?
Time Dependent Monotonic (Creep) Mechanical Properties	ASTM E139 - 06 Standard Test Methods for Conducting Creep, Creep-Rupture, and Stress-Rupture Tests of Metallic Materials	Yes	With Modifications
	ASTM E328 - 02 (2008) Standard Test Methods for Stress Relaxation Tests for Materials and Structures	Yes	With Modifications
	ASTM E1457 - 07e1 Standard Test Method for Measurement of Creep Crack Growth Times in Metals	Yes	With Modifications

Table 6.17 Time Dependent Mechanical Testing

#### 6.3.4 Cyclic Mechanical Properties (Isothermal)

Cyclic (isothermal) test data is used to validate the model constitutive equation. The test temperatures, strain rates, and strain limits bound the interconnection service and test environments. The starting and ending microstructures should be documented by metallographic cross section techniques.

The data required from these tests illustrate the hysteresis loops, strain energy, and percent load-change (drop or rise) as a function of cycle. All solder compositions can be evaluated by the ASTM test methods listed in Table 6.18. As with the prior tests, modifications to the sample geometry and test fixture are required for test specimens having size scales equivalent to the microstructure.

6. Testing

Baseline Practice	Test and Applicable Standard	Is the Current Test Equipment Adequate for Pb-Free?	Are the Current Test Parameters Adequate for Pb-Free?
Cyclic Mechanical Properties (Isothermal)	ASTM E606 - 04e1 Standard Practice for Strain-Controlled Fatigue Testing	Yes	With Modifications
	ASTM E468 - 90 (2004) e1 Standard Practice for Presentation of Constant Amplitude Fatigue Test Results for Metallic Materials	Yes	With Modifications

Table 6.18 Cyclic Mechanical Testing

6.3.5 Material Physical Properties

The critical physical property required by the computational model is the coefficient of thermal expansion. The CTE is measured over the temperature range expected of both test and service lifetime environments. The starting and ending microstructures should be documented by metallographic cross section techniques. All solder compositions can be evaluated by the ASTM test methods listed in Table 6.19. Modifications to the sample geometry and test fixture are required to test the material at size scales equivalent to the microstructure.

Baseline Practice	Test and Applicable Standard	Is the Current Test Equipment Adequate for Pb-Free?	Are the Current Test Parameters Adequate for Pb-Free?
Material Physical Properties	ASTM E831 - 06 Standard Test Method for Linear Thermal Expansion of Solid Materials by Thermomechanical Analysis	Yes	With Modifications
	ASTM E289 - 04 Standard Test Method for Linear Thermal Expansion of Rigid Solids with Interferometry	Yes	With Modifications



Baseline Practice	Test and Applicable Standard	Is the Current Test Equipment Adequate for Pb-Free?	Are the Current Test Parameters Adequate for Pb-Free?
	ASTM E228 - 06 Standard Test Method for Linear Thermal Expansion of Solid Materials with a Push-Rod Dilatometer	Yes	With Modifications
	ASTM E1545 - 05 Standard Test Method for Assignment of the Glass Transition Temperature by Thermomechanical Analysis	Yes	With Modifications

Table 6.19 Physical Property Testing

6.3.6 Failure Mode Analysis of Materials Test Specimens

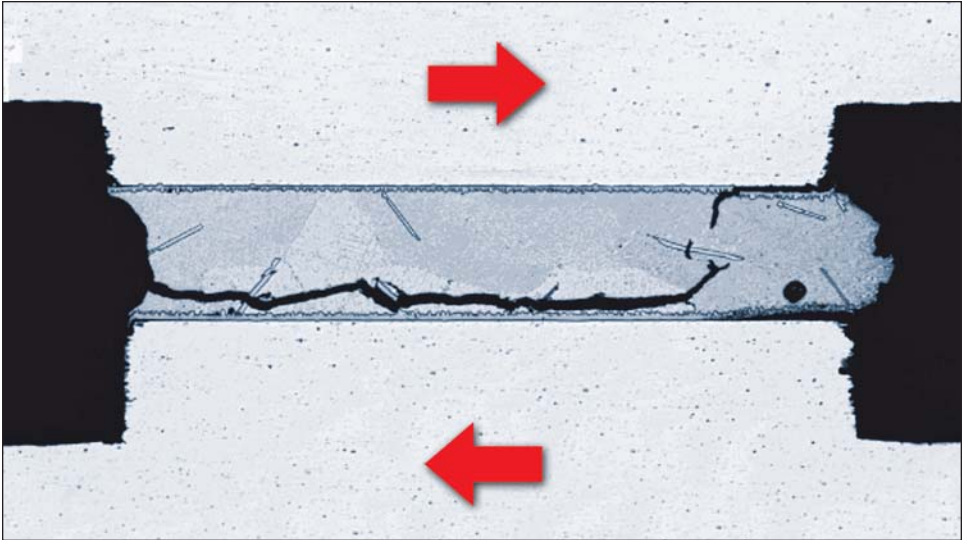
A thorough failure mode analysis is performed after testing using metallographic cross sections to reveal the post-test microstructure, and scanning electron microscopy to assess fracture surfaces. Traditional metallographic cross sectioning techniques are used with consideration paid to the softer solder materials. Essentially, no change in current micro-sectioning techniques is required, but in some cases a focused ion beam (FIB) technique may be necessary to see some features.

Baseline Practice	Test and Applicable Standard	Is the Current Test Equipment Adequate for Pb-Free?	Are the Current Test Parameters Adequate for Pb-Free?
Failure Mode Analysis of Materials Test Specimens	IPC-TM-650, Method 2.1.1 Rev. E, "Micro-sectioning, Manual Method," May 2004	Yes	Yes

Table 6.20 Failure Analysis

6.3.7 Simulated Solder Joint Testing

The testing of simulated Pb-free solder joints provides yield and failure strength data as well as early validation of the computational model.



**Figure 6.3** *Lap Shear Simulated Solder Joint*

The test conditions should bound product test and service conditions: temperatures, strain ranges, strain rates, and applied stresses (tension, compression, or shear). It is necessary to perform metallographic cross sections of the samples prior to testing to document the initial microstructure, including void formation.

There are no standardized tests for any solder joints. The ASTM test methods for adhesive joints are most relevant for solder joints; they are listed below and referenced to Table 6.21. The solder joint geometry (footprint and gap thickness) must be clearly defined and should consider the microstructure size scale effects. It is critical that the compliance of the load train be fully taken into account in order to correctly analyze and interpret the data. The tests for the simulated solder joint are:

- Time Independent Monotonic (Stress-Strain) Mechanical Properties, which includes ASTM D3165-07, and ASTM D3528-96
- Time Dependent Monotonic (Creep) Mechanical Properties (ASTM D2294-96 and ASTM D2293-96)
- Cyclic Mechanical Properties (Isothermal)

Baseline Practice	Test and Applicable Standard	Is the Current Test Equipment Adequate for Pb-Free?	Are the Current Test Parameters Adequate for Pb-Free?
Time Independent Monotonic (Stress Strain) Mechanical Properties	ASTM D3165 - 07 Standard Test Method for Strength Properties of Adhesives in Shear by Tension Loading of Single-Lap-Joint Laminated Assemblies	Yes	No
	ASTM D3528 - 96 (2008) Standard Test Method for Strength Properties of Double Lap Shear Adhesive Joints by Tension Loading	Yes	No
Time Dependent Monotonic (Creep) Mechanical Properties	ASTM D2294 - 96 (2008) Standard Test Method for Creep Properties of Adhesives in Shear by Tension Loading (Metal-to-Metal)	Yes	No
	ASTM D2293 - 96 (2008) Standard Test Method for Creep Properties of Adhesives in Shear by Compression Loading (Metal-to-Metal)	Yes	No
Cyclic Mechanical Properties (Isothermal)	No Industry Standard Test Method Exists	Yes	No

Table 6.21 Simulated Solder Joint Testing

### 6.3.8 Failure Mode Analysis of Simulated Solder Joints

Simulated solder joint testing must be followed by failure mode analysis of the Pb-free solder joints. Scanning electron microscopy is performed on the fracture surfaces, followed by metallographic cross sections. Traditional metallographic cross sectioning techniques are applicable, therefore little or no change in current micro-sectioning techniques are required. Focused ion beam techniques may be required to see some features.

6. Testing

Baseline Practice	Test and Applicable Standard	Is the Current Test Equipment Adequate for Pb-Free?	Are the Current Test Parameters Adequate for Pb-Free?
Failure Mode Analysis of Simulated Solder Joints	IPC-TM-650, Method 2.1.1 Rev. E, "Microsectioning, Manual Method," May 2004	Yes	Yes

Table 6.22 Failure Analysis of Simulated Solder Joints

Issues/Gaps/Misconceptions

- Gap: There is an absence of consistent mechanical and physical properties data from current and newly-developed Pb-free solders, which can support the fidelity needed from computational model predictions of associated interconnections.
- Gap: There is a need to determine the rate kinetics of those micro-structural processes that underlie the stabilization process in Pb-free solder (Section 6.2.1).
- Gap: In general, there are no standardized tests for simulated solder joints (Section 6.2.7).
- Gap: There is little test data and no standardized specimen geometries and test methods for evaluating the effects of Pb-free solder specimen size vis-à-vis microstructure on the mechanical and physical properties of the interconnections (Sections 6.2.2, 6.2.3, and 6.2.5).
- Gap: Due to their softness, Pb-free alloys require additional precautions during handling and/or performing failure mode analysis (Sections 6.2.6 and 6.2.8).

Conclusions

Computational modeling provides a cost-effective means to predict the fatigue performance of Pb-free solder interconnections.

Computational models are necessary to determine hardware test parameters for verification, validation, acceptance, or qualification of Pb-free solder joints based on service life requirements.

Optimizing the fidelity of computational model predictions requires accurate mechanical and physical properties of the Pb-free solder alloys to serve as input and validation data.

Recommendations

High fidelity computational models must be developed for accurately predicting the fatigue lifetime of Pb-free solder joints.

A database of accurate materials mechanical and physical properties must be compiled to provide both input and validation data for those computational models.

6.4 CIRCUIT CARD ASSEMBLY TESTING  
(TEST VEHICLES AND PRODUCTION HARDWARE)

Current Baseline Practice

This section covers testing of test vehicles for measuring robustness of solders and other Pb-free materials, and for qualifying processes. These tests are often conducted to the point of failure so that reliability comparisons can be made. This section also covers testing of production hardware methods which can be used for ESS, verification, validation, acceptance, and qualification tests. These tests simulate one or more hardware lifetimes in an effort to determine the degree and type of failures that occur. The actual parameters (temperature extremes, dwell times, Power Spectral Densities (PSD), etc.) used for each test will be determined by system requirements.

6.4.1 Humidity Testing

Currently used test methods and equipment (MIL-STD-810G, Method 507.5) are adequate for humidity testing of Pb-free test vehicles. Actual test parameters will be defined by the system requirements.

Baseline Practice	Test and Applicable Standard	Is the Current Test Equipment Adequate for Pb-Free?	Are the Current Test Parameters Adequate for Pb-Free?
Humidity Testing	MIL-STD-810G, Method 507.5, "Environmental Engineering Considerations and Laboratory Tests," October 31, 2008	Yes	Yes

Table 6.23 Humidity Testing

## 6. Testing

### 6.4.2 Thermal Shock

Currently used test methods and equipment (MIL-STD-810G, Method 503.5) are adequate for thermal shock testing of Pb-free test vehicles to failure. Thermal shock is defined as a temperature change rate of 20 °C/minute (or greater). IPC-SM-785 cautions that thermal shock cycling is not a substitute for thermal cycling because it can induce failure mechanisms not seen in thermal cycling, due to warping of the test vehicle. IPC-SM-785 recommends that thermal shock cycling only be used if the intent is to simulate a thermal shock environment.

Baseline Practice	Test and Applicable Standard	Is the Current Test Equipment Adequate for Pb-Free?	Are the Current Test Parameters Adequate for Pb-Free?
Thermal Shock	MIL-STD-810G, Method 503.5, "Environmental Engineering Considerations and Laboratory Tests," October 31, 2008	Yes	No

Table 6.24 Thermal Shock

### 6.4.3 Thermal Cycling

Currently used test methods and equipment (IPC-SM-785 and IPC-9701) are adequate for thermal cycle testing of Pb-free test vehicles to failure and for ESS, verification, validation, acceptance, and qualification thermal cycle testing of Pb-free production hardware.

A thermal cycle of -55 °C to +125 °C with dwell times of 10-15 minutes is commonly used by A&D. The thermal cycle parameters (temperature extremes, dwell times, and ramp rates) for testing test vehicles to failure will vary depending upon the goals of the test and the resources available to conduct the testing. As a default Pb-free test condition, IPC-9701 suggests the use of a 0 to +100 °C temperature cycle with either a 10 minute or a 30+ minute dwell "depending on the reliability approach and user need." If models exist, the test results can be converted into field lifetimes (IPC-SM-785 and IPC-9701).

For production hardware, the choice of thermal cycle test parameters (temperature extremes, ramp rates, and dwell times) should be chosen so that the test is equivalent to a specific time in the field. This will require computational models that can convert the expected field conditions into accelerated test conditions.

Baseline Practice	Test and Applicable Standard	Is the Current Test Equipment Adequate for Pb-Free?	Are the Current Test Parameters Adequate for Pb-Free?
Thermal Cycling (For ESS, Verification, Validation, and Qualification Testing)	IPC-SM-785, "Guidelines for Accelerated Reliability Testing of Surface Mount Solder Attachments," November 1992	Yes	No
	IPC-9701A, "Performance Test Methods and Qualification Requirements for Surface Mount Solder Attachments," February 2006	Yes	No
	GEIA-STD-0005-3, Performance Testing for Aerospace and High Performance Electronic Interconnects Containing Pb-free Solder and Finishes, June 2008	Yes	No

Table 6.25 Thermal Cycling

6.4.4 Vibration Testing

Currently used test methods and equipment are adequate for vibration testing of Pb-free test vehicles to the failure point, and for ESS, verification, validation, acceptance, and qualification vibration testing of Pb-free production hardware (MIL-STD-810G, Method 514.6). The PSD input parameters for testing test vehicles to failure will vary depending upon the goals of the test and the resources available to conduct the testing.

The PSD input parameters for testing of production hardware will be based on the individual system requirements. The choice of vibration test parameters (PSD levels and test durations) should be chosen so that the test is equivalent to a specific time in the field. This will require computational models that can convert the expected field conditions into accelerated test conditions.

6. Testing

Baseline Practice	Test and Applicable Standard	Is the Current Test Equipment Adequate for Pb-Free?	Are the Current Test Parameters Adequate for Pb-Free?
Vibration Testing (For ESS, Verification, Validation, and Qualification Testing)	MIL-STD-810G, Method 514.6, "Environmental Engineering Considerations and Laboratory Tests," October 31, 2008	Yes	No

Table 6.26 Vibration Testing

6.4.5 Mechanical Shock Testing

Currently used test methods and equipment are adequate for mechanical shock testing of Pb-free test vehicles to failure point and for ESS verification, validation, acceptance, and qualification mechanical shock testing of Pb-free production hardware (MIL-STD-810G, Method 516.6). The shock pulse or Shock Response Spectrum (SRS) input parameters for testing test vehicles to failure will vary depending on the goals of the test.

The shock pulse or SRS input parameters for testing production hardware will be defined by the individual system requirements. Since SAC solders are less robust than SnPb solder under shock loading, the use of stiffeners on the circuit boards or the use of shock isolators on the boxes holding the circuit assemblies may be required to increase the reliability of the CCAs.

Baseline Practice	Test and Applicable Standard	Is the Current Test Equipment Adequate for Pb-Free?	Are the Current Test Parameters Adequate for Pb-Free?
Mechanical Shock Testing (For Verification, Validation, and Qualification Testing)	MIL-STD-810G, Method 516.6, "Environmental Engineering Considerations and Laboratory Tests," October 31, 2008	Yes	No
	IPC/JEDEC-9703, "Mechanical Shock Test Guidelines for Solder Joint Reliability," March 2009	Yes	No

Table 6.27 Mechanical Shock Testing



6.4.6 Isothermal Aging

Appropriate aging of SAC solder joints before conducting testing may be essential in order to ensure that the solder has the metallurgy and mechanical properties of a solder aged several years in the field.

IPC-9701 recommends that solder joints on test vehicles should be subjected to accelerated thermal aging (e.g., 24 hours at 100 °C) in air to accelerate processes such as solder grain growth, intermetallic compound growth, and oxidation in order to yield metallurgy similar to that seen after aging in the field. The optimum conditions for thermal aging of Pb-free solder alloys prior to testing have yet to be established.

Baseline Practice	Test and Applicable Standard	Is the Current Test Equipment Adequate for Pb-Free?	Are the Current Test Parameters Adequate for Pb-Free?
Isothermal Aging	No Industry Standard Test Method Exists	No	No

Table 6.28 Isothermal Aging

6.4.7 Combined Environments (HALT, HAST)

Some commonly used tests combine two or more environments into one test. For example, HALT does random repetitive shock and thermal cycling at the same time. HAST combines high temperature, humidity and pressure (power-on or power-off). Currently used test methods and equipment (GMW8287 and JESD22-A110C) are adequate for HALT and HAST testing of Pb-free test vehicles to failure.

Validated computational models for converting combined environment test results into field lifetimes probably do not exist. Therefore, HALT is best used as a screening test for uncovering defects and weak spots in production hardware and not as a tool for determining reliability. HALT PSD inputs are often not well characterized which means that the resonance frequencies of the test article can be excited more (or less) than anticipated, resulting in unintentional over-testing (or under-testing) of the test article.

6. Testing

Baseline Practice	Test and Applicable Standard	Is the Current Test Equipment Adequate for Pb-Free?	Are the Current Test Parameters Adequate for Pb-Free?
Combined Environments (HALT, HAST)	GMW8287, "Highly Accelerated Life Testing," February 1, 2002	Yes	No
	JESD-22-A110C, "Highly Accelerated Temperature and Humidity Stress Test (HAST)," January 2009	Yes	No

Table 6.29 Combined Environmental Testing

6.4.8 Electromigration Testing

As the size of solder joints decrease (e.g., the diameter of solder balls is approaching 50 microns), electromigration may become a reliability issue due to void and intermetallic formation [1, 2]. No standardized test method exists for conducting this testing.

Baseline Practice	Test and Applicable Standard	Is the Current Test Equipment Adequate for Pb-Free?	Are the Current Test Parameters Adequate for Pb-Free?
Electromigration Testing (Small Solder Balls)	No Industry Standard Test Method Exists	No	No

Table 6.30 Electromigration Testing

6.4.9 Failure Mode Analysis of Test Vehicles

No change in current micro-sectioning techniques is required (IPC-TM-650, Method 2.1.1 Rev. E). Focused ion beam techniques may be required to see some features.

- Black Pad, Kirkendall Voids, Pad Cratering, Pad Lifting, Trace Cracking

There are no current standardized test methods. A pad cratering test is in development [3].

Baseline Practice	Test and Applicable Standard	Is the Current Test Equipment Adequate for Pb-Free?	Are the Current Test Parameters Adequate for Pb-Free?
Failure Mode Analysis of Test Vehicles	IPC-TM-650, Method 2.1.1 Rev. E, "Microsectioning, Manual Method," May 2004	Yes	Yes
Black Pad, Kirkendall Voids, Pad Cratering, Pad Lifting, Trace Cracking	No Industry Standard Test Method Exists	No	No

Table 6.31 Failure Analysis of Test Vehicles

### Issues/Gaps/Misconceptions

- Issue: Pb-free solders are less robust than SnPb in vibration and mechanical shock.
- Gap: Validated computational models will be needed to convert data from accelerated tests into field lifetimes and also to design hardware qualification tests that are equivalent to one or more field lifetimes.

### Conclusions

Current test methods and equipment do not need to be changed. Test parameters will be supplied by the system requirements.

Validated computational models are needed to relate test parameters to service life conditions.

### Recommendations

Develop new test standards where none exist (e.g., isothermal aging) and modify existing standards with appropriate test parameters (e.g., vibration PSD) for Pb-free assemblies.

Validated computational models need to be developed to convert data from accelerated tests into field lifetimes, and also to design hardware qualification tests that are equivalent to one or more field lifetimes. Detailed information on test vehicle design, test parameters, and the response of test vehicles must be generated for model development.

“Personally I’m always ready to learn,

although I do not always like being taught.”

—Sir Winston Churchill (1874-1965)



photo courtesy of MaudMaven / T.S. Heide

# 7. Reliability

## 7.1 INTRODUCTION

The introduction of Pb-free materials and processes (LFM&P) into A&D electronics systems and products will significantly affect the ability to predict and verify reliability. The causes of this include:

- Incompletely characterized materials.
- Wider and changing suite of materials.
- Immature processes with narrower process windows.
- Intrinsic complexities of the physical properties and metallurgy of Pb-free solders.

These factors currently confound the ability to model and interpret test results, and therefore limit the confidence in the methods used to predict reliability.

### 7.1.1 Reliability Program Activities

Reliability programs are required to ensure that systems perform their intended function over their intended lifetime and in their intended usage environment. Nearly all A&D programs specify reliability requirements that include metrics germane to the particular system application, and under specific service life cycle conditions. Top-level system reliability and associated environmental requirements are converted into a set of derived requirements for subsystems. It is not anticipated that the standard methodologies currently employed in this flow down process will require modification as a result of the introduction of Pb-free materials and processes.

It is standard practice for A&D programs to have a formal reliability program in place to ensure that appropriate activities occur in all lifecycle phases, and to establish that the overall reliability requirements are satisfied. The flow of reliability interaction with the product life cycle is depicted in Figure 7.1.

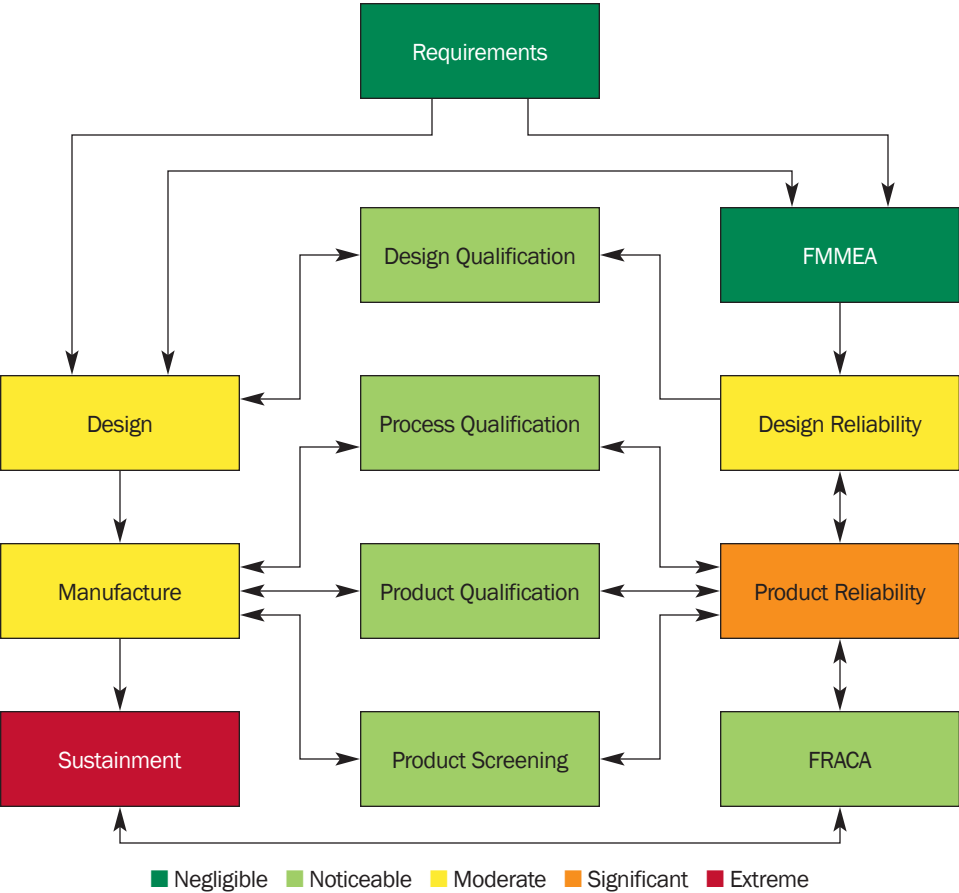


Figure 7.1 Basic elements of a reliability program. The color coding reflects the expected relative impact of LFM&P on each portion of the reliability program.

The form and structure of reliability programs are not expected to change. It is a common requirement that various forms of reliability predictions be performed for A&D systems. System level reliability predictions are typically performed in accordance with standards such as MIL-HDBK-217, which is

not recommended as a best practice in IEEE-1413.1, and has not been updated in over a decade. This document is completely out of step with the majority of electronic devices being fielded today, and does not consider LFM&P at all.

Recently introduced GEIA-STD-0009 requires an understanding of failure sources in predicting system level reliability. The LEAP-WG is preparing a document (GEIA-HDBK-0005-4) that is intended to provide guidance for the performance of reliability assessments of A&D systems incorporating LFM&P. It is recommended that these documents serve as a basis for the implementation of improved practices, and that the team working on this document continue to be supported to perform future updates and refinements.

Once a system has moved past design into manufacturing and integration, new reliability tasks of verification tracking begins to take place. The overall structure of these program elements is not anticipated to require modification to accommodate the needs of LFM&P. Specific test conditions employed for qualification and screening may not necessarily change, but the interpretation of test results need to be re-examined. Material testing based on LFM&P must be supported to inform these interpretations. Ultimately, reliability must focus on the impact of LFM&P on failure mechanisms and dominant sources of failure, which are discussed in this section.

Tracking and reporting of failures should be able to proceed as with SnPb product. Enhanced tracking of pilot runs of Pb-free products will be required, however, to maximize the value of these tests.

### 7.1.2 Failure Modes and Mechanisms

It is necessary to have an understanding of the applicable failure modes and mechanisms, as well as models, in order to make meaningful predictions and to perform meaningful tests. The remainder of this section provides detailed information on each of the principal hardware failure mechanisms affecting soldered A&D assemblies.

Reliability failures are divided into early (infant), random (in use), and wearout (end-of-life) classes. The total failure rate as a function of time is represented by the sum of these three subsets. This notion is typically exemplified by the so-called “bathtub curve,” which is illustrated in the following figure.

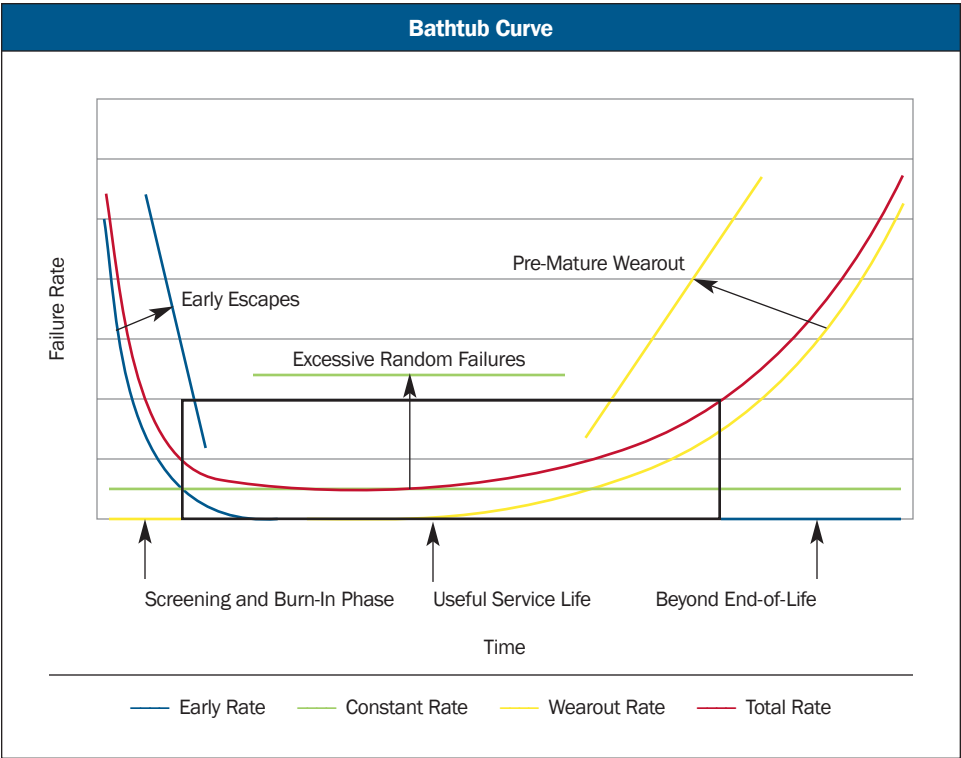


Figure 7.2 Bathtub curve illustrating how the three classes of failure modes affect system level reliability over the entire lifecycle.

Early failures are the result of manufacturing or material defects. The principal tools used to control these failures are inspection and screening tests. Improper control of these failures results in the left hand side of the bathtub curve moving out to the right, thereby affecting the failure rate of the product in the field during the first portion of its life. This excess unreliability persists until such time that the affected population falls out through failure or removal.

Wearout failures are also often referred to as “end-of-life” failures. The principal tools used to control these failures are life testing and associated modeling. Improper control of this class of failures results in the right-hand side of the bathtub curve shifting leftward. The result of this is that the unreliability of the system increases prematurely and it may become unusable before completing the required service life.



Random or in-use failures result from defects escaping design and manufacture, early wearout failures, as well as unanticipated changes in use conditions. The in-use failure rate is often represented as being constant over time, which manifests itself as a steady-state *mean time between failure* (MTBF) over the service life of the system. Random failure modes are controlled through a variety of processes, with a robust failure reporting and corrective action (FRACA) process being chief among them.

Each of the specific failure sources discussed in detail below is summarized in the following table. It is intended to provide a snapshot of the impact of LFM&P on the most important failure sources, and the adequacy of the Current Baseline Practices employed to manage these failure sources. Also within the table, each failure is assigned to one of the three portions of the bathtub curve so as to illustrate the potential impact on system level reliability.

Site	Failure Source	Mode	Stage	Primary Driver	Management	Impact of Lead Free	Repair/ Rework Impact	Risk with Current Best Practice
Solder Joint	Manufacturing Defects	Shorts/ Opens	Early	Mechanical Loads	Inspection/ Screen	Medium	High	Medium
Solder Joint	Thermal Cycle Fatigue	Opens	End-of-Life	Temperature	Test/Model	Medium	Medium	Medium/ High
Solder Joint	High Cycle Vibration Fatigue	Opens	End-of-Life	Vibration	Test/Model	Medium	Medium	Medium
Solder Joint	Shock/Low Cycle Vibration Fatigue	Opens	End-of-Life	Shock/ Vibration	Test/Model	High	High	Medium
Solder Joint	Combined Environments	Shorts/ Opens	End-of-Life	Temperature/ Vibration	Test/Model	High	High	High
Solder Joint	Mixed Solders	Shorts/ Opens	Random	Temperature/ Vibration	Test/Model	High	High	High
Solder Joint	Underfill	Opens	End-of-Life	Temperature	Test/Model	Medium	Medium	Medium
Solder Joint	Low Temperature Brittle Fracture	Opens	End-of-Life	Shock/ Vibration	Test	Medium	Medium	Medium
Solder Joint	Creep Rupture	Opens	End-of-Life	Temperature/ Mechanical Load	Test/Model	High	Medium	High
Solder Joint	Electromigration	Opens	End-of-Life	Current Density	Test/Model	Medium	Medium	Medium
Solder Joint	Tin Pest	Opens	Random	Temperature	Test	Medium	Low	Low

## 7. Reliability

Site	Failure Source	Mode	Stage	Primary Driver	Management	Impact of Lead Free	Repair/ Rework Impact	Risk with Current Best Practice
PWB	Manufacturing Defects	Shorts/ Opens	Early	Temperature/ Vibration/ Humidity	Inspection/ Screen	High	High	Medium
PWB	Barrel Cracks	Opens	End-of-Life	Temperature	Test/Model	Medium	High	Low
PWB	Trace Fatigue Cracks	Opens	End-of-Life	Temperature/ Vibration/ Shock	Test/Model	Medium	High	Low
PWB	Pad Cratering	Opens	Early/ End-of-Life	Temperature/ Vibration/ Shock	Test	High	High	Medium
PWB	Conductive Anodic Filament	Shorts	Early	Voltage/ Humidity	Test/Model	High	High	Medium
PWB	Creep Corrosion and Dendritic Growth	Shorts	Random/ End-of-Life	Corrosive Atmospheres	Test	Medium	Medium	Medium
Assembly	Tin Whiskers	Shorts	Random	Varied	Test/Model	High	Low	Medium
Components	Temperature Sensitivity	Shorts/ Opens	Early	Temperature	Inspection/ Screen	High	High	Medium
Components	BGA CTE and Warpage	Opens	Early	Temperature/ Vibration	Inspection/ Screen	Medium	High	Medium
Components	Plastic Component Delamination	Opens	Early	Humidity/ Temperature/ Vibration	Inspection/ Screen	Medium	Medium	Low

Table 7.1 Failure sources and their relationship to the reliability of Pb-free A&D systems.

### 7.1.3 Rework and Repair Effects

Rework and repair activities play a significant role in the manufacture and sustainment of A&D systems. LFM&P will have a significant impact on rework and repair activities which are expected to impact reliability. From this perspective, a more disciplined approach and deeper understanding of rework/repair will be needed. The severity of the interaction between failure sources and rework/repair is highlighted in Table 7.1 above.

## 7.2 FAILURE SOURCES

### 7.2.1 Solder Interconnections

Solder interconnects are required to provide electrical and mechanical connections between packaged devices and large connection structures, most commonly, the printed wiring board. One of the most obvious impacts to A&D products due to supply chain adoption of RoHS materials is the change from a SnPb solder to a Pb-free solder. While a wide variety of Pb-free solders exist and more are being developed, tin-silver-copper (SAC) and tin-copper solder have been selected and are now widely used by the consumer and commercial industry. For tin-silver-copper solders, SAC305 and SAC405 have received the most significant amount of study with SAC305 taking the lead. For wave solder, the copper dissolution issue has been primarily responsible for SAC305 losing ground to tin-copper; usually in the form of tin-copper-nickel.

To date, a significant amount of research has been invested in temperature cycling performance of Pb-free solders. Recently, attention has shifted to shock durability as consumer adopters found issues with drop shock reliability in hand-held applications. Acceleration and time to failure models based on material science and SnPb solder have been published, but their ability to predict field life has not been verified.

This section provides a discussion of the solder interconnect failure sources. It is divided into loading conditions which occur during the life and testing of the solder joint, with special consideration to interconnects formed by combining solders of differing composition, which occurs with attachment of ball grid array packages.

#### *Manufacturing Defects*

Improper manufacturing processes can result in improperly formed or damaged solder interconnects. These compromised solder interconnects can lead to both early and elevated random failures. The identification and sources of defects in SnPb solder interconnects are well documented and controlled by the design and manufacturing processes. LFM&P introduces an elevated risk for defects that can only be resolved by cooperation between reliability, manufacturing, and design. Current Pb-free solders require higher assembly temperatures of 20°C or more compared to those used for SnPb solder assembly. This results in higher rates for intermetallic formation and greater deformations, which when uncontrolled, will result in increased levels of defects. Many of these defects have been identified by advanced product development teams and it is critical that manufacturing develop and qualify practices to control them. Some defects can be identified by inspection processes while others may have to be removed by stress screens.

## 7. Reliability

---

- Current Baseline Practice

Non-destructive inspection is used to identify gross defects such as poorly formed joints, starved joints, tombstoning, and high contact angles. Area array technology requires x-ray inspection for voiding, missing solder connections, starved joints, and bridging. Current inspection protocols are identified in industry standards such as IPC-610D and IPC-7095. In addition, destructive analysis of assembly samples may be used to verify proper joint formation. Environmental stress screens are commonly used to precipitate failure of defective solder interconnects. All of these procedures are impacted by conversion to Pb-free solder.

- Issues/Gaps/Misconceptions

Surface inspections are not sufficient to identify all interconnect defects. Due to material composition, the surface appearance of SAC solders may be grainy and shrink cracks may occur. For SAC ball grid arrays assembled with SnPb solder, the solder surface appearance and x-ray inspection are insufficient to determine joint reliability.

ESS reduces the life of a solder interconnect, requiring balance between capturing defective solder interconnects versus reducing the life of properly formed solder joints. In development, it is important to verify that a sufficient life margin remains after ESS (see *Combined Loading* later in this section).

- Conclusions and Recommendations

It is critical that the assembly manufacturers develop qualified processes that eliminate or control defect levels. Mixed solder cannot be discerned by the normal inspection processes. Therefore, solder composition of BGA spheres must be tightly controlled.

### *Interconnect Fatigue*

Solder interconnects may fail by wear out (fatigue) under high cycle (vibration) or low cycle (thermal cycling, repetitive shock) conditions, or due to a single overstress event (shock). The microstructure and damage evolution in mainstream Pb-free solders differ significantly from SnPb solders. Thus, for example, effects of Sn grain orientation lead to significant scatter in fatigue resistance, strength, and creep properties [1-4], so that the most stressed (corner) joint is not necessarily the first that fails. Additionally, there tends to be more incidences of early failures. Models and *rules of thumb*

for evaluating life expectancy of interconnects, under anticipated life cycle loads which worked for SnPb, may not be appropriate for mainstream lead free solders. As a further complication, LFM&P can weaken laminate interfaces, resulting in pad cratering.

### Temperature Cycling

Temperature excursions arising from operation and environmental conditions are known to limit the life of CCAs and need to be assessed based on the design requirement. Temperature cycling has been one of the most intensely studied topics related to LFM&P. For relatively small temperature excursions in the range of 0 to 100 °C with low to moderate ramp rates and short dwell times, the performance of SAC305/405 has been shown to be far superior to SnPb. For a wider range, such as -55 to 125 °C and longer dwell times, the fatigue life of SAC305/405 is further reduced and may end up slightly shorter than for SnPb, depending on package type. Fatigue life models have been derived and a significant set of test data generated over the past ten years.

- Current Baseline Practice

The life expectancy of solder interconnects under use conditions is assessed in design through models and/or validated through qualification tests. The latter requires acceleration factors or *rules of thumb* to determine the level of testing required to verify that wearout failures will not occur in use. An acceleration factor (AF) is defined as

$$AF = \frac{N_{use}}{N_{test}}$$

where  $N_{use}$  is the time or cycles to failure in use and  $N_{test}$  is the time or cycles to failure in test. For SnPb, industry standards such as IPC-9701, reference the so-called “Engelmaier Model” [5-7]. In addition, a number of temperature cycle fatigue failure modeling approaches have been developed and documented in the literature [8-20]. Many of these approaches require detailed finite element modeling, but the “Engelmaier Model” [9, 14, 15], the SRS model [11], and the Norris Landzberg model [8, 17, 18] – originally developed by IBM for C4 technology – do not. The latter is, in fact, not a true fatigue life model but only predicts acceleration factors. In general, the fatigue models are based on the Manson-Coffin or Morrow models, which relate the number of cycles to failure,  $N_f$ , to cyclic strain range,  $\Delta\gamma$ , or cyclic strain energy,  $\Delta W$ . Some of the prevalent models are identified in Table 7.2.

7. Reliability

Model	Model Form	Requires FEA	Model Constants Available for SnPb	Model Constants Available for Pb-Free (SAC305)
IPC-9701 (Engelmaier [9,13,14])	$N_f = \frac{1}{2} \left( \frac{\Delta \gamma}{2 \epsilon_f} \right)^{\frac{1}{c}}$	No	Yes	Yes
SRS (Clech [11])	$N = C_1 (\Delta W)^{d_1}$	No	Yes	Yes
Norris Landzberg [8,17-19])	$AF = \left( \frac{f_f}{f_i} \right)^{-m} \left( \frac{\Delta T_f}{\Delta T_i} \right)^{-n} \exp^{\frac{E_a}{K} \left( \frac{1}{T_f} - \frac{1}{T_i} \right)}$	No	Yes	Yes
Inelastic Energy (Schubert [16])	$N = C_2 (\Delta W)^{d_2}$	Yes	Yes	Yes
Energy Partitioning (Dasgupta [10])	$\begin{aligned} \text{Energy} &= U_e + W_b + W_{cr} \\ &= U_o N_{je}^{b'} + W_{po} N_{jp}^{c'} + W_{co} N_{jc}^{d'} \end{aligned}$	Yes	Yes	Yes
Strain Energy (Syed [12])	$Nf = (0.02 E_{GBS} + 0.063 E_{MC})$	Yes	Yes	Yes

Table 7.2 Temperature Cycle Fatigue Models

- Issues/Gaps/Misconceptions  
Existing SnPb solder reliability models suffer from a variety of issues but have been accepted due to the long use of SnPb solders. Clearly our predictive experience with Pb-free solder interconnect reliability, lacks the maturity of the knowledge ascertained over the years with predicting SnPb interconnect reliability.

For Pb-free solders, the influence of process parameters, solder volume, long term aging, mixed alloys and load history are not adequately addressed or are simply ignored by existing models. These omissions raise serious concerns over the ability of existing models to predict long-term life performance.

For instance, many BGA packages are available with solder balls of low-silver and quaternary alloys that may improve drop shock behavior. However, these alloys may have significantly negative influences on temperature cycling performance, and currently, we cannot directly account for these mixed alloys in fatigue life between test and field.

Limited isothermal aging led to clear reductions in the thermal cycling fatigue life of large SAC305 joints [23, 24]. Smaller joints, lower silver content, and longer aging are all expected to show a greater sensitivity, but this has yet to be quantified. Overall, micro-structural aging is not understood well enough and short term high temperature aging (1000 hours @ 125°C) does not necessarily represent a worst case simulation of effects which may occur after even a few years of operation (Appendix).

Linear damage accumulation is invariably assumed when predicting the performance of Pb-free solder interconnects subject to the non-uniform temperature excursions commonly experienced by fielded electronics. However, this has yet to be justified (see *Combined Loading*).

Material properties of mainstream Pb-free solders, such as creep, have been demonstrated to change dramatically over time.

Finally, even relative comparisons (ranking) of assembly life may depend on the dwell time used in accelerated testing (Appendix). This result suggests significant consequences for design, materials, and process optimization.

- **Conclusions and Recommendations**

Reliability programs should be advised that the level of maturity for fatigue life estimation of mainstream Pb-free materials is not at the level of SnPb solder. In addition, the combined effects of aging, alloy mixing, and variations in environmental profile may lead to significant errors in *model predicted* life expectancy. These combined effects may result in acceleration factor errors of five to ten times or more, while further failure mechanisms may be different depending on service conditions (Appendix).

It is recommended to place Pb-free assemblies in the field under a variety of environments and non-critical applications as soon as possible. This is the only means of generating the field experience that will be necessary to validate models.

Research into aging effects, failure mechanisms, mixed Pb-free alloys, and damage accumulation to improve existing or developing new models, should be supported.

## 7. Reliability

### Vibration (High Mechanical Cycle)

During their life cycle, A&D products are commonly subjected to a wide range of application-specific vibration. *Vibration induced* board curvature results in cyclic strains in the solder joints, but unlike temperature cycling, the loading is highly dependent upon component location and the numbers of cycles are characteristically an order of magnitude higher. SnPb solder interconnects were typically tested under severe load levels and issues arising from test were mitigated through the addition of stiffeners and bonding materials. For certain package types, mainstream Pb-free solders have demonstrated a lower durability than SnPb under elevated vibration levels. In addition, failures arising under high vibration levels are not limited to solder cracking but have included both trace failure and pad cratering. Figure 7.3 depicts a typical solder crack in a SAC joint, and Figure 7.4 reveals a vibration induced trace failure. Like SnPb, Pb-free solders will require mitigation to survive elevated vibration and shock loading. At present, insufficient testing has been conducted to validate simulation models and provide *rules of thumb* for when vibration mitigation must be applied.

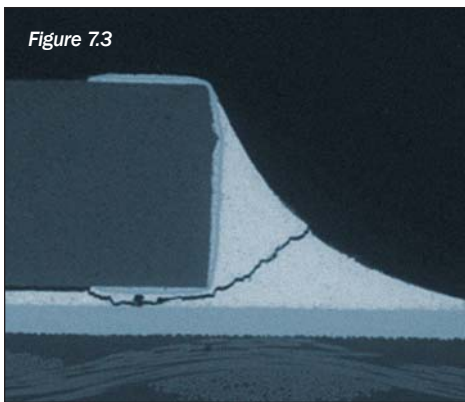


Figure 7.3 Vibration induced solder fillet failure. Courtesy CALCE, UMD.

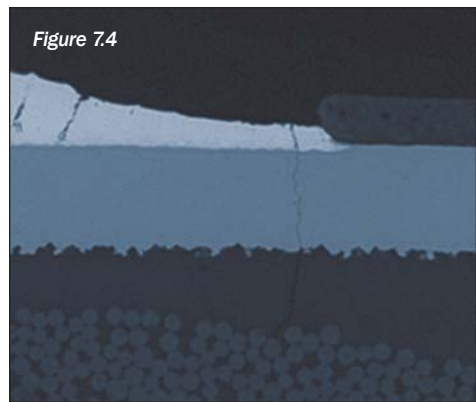


Figure 7.4 Vibration induced trace failure. Courtesy CALCE, UMD.

- Current Baseline Practice

For applications with significant vibration life cycle loading, a designer will need to carefully consider part positioning and may need to intrinsically design for mitigation earlier than previously used with SnPb. Finite element models may be used to determine *vibration induced* board strain history. Additional finite element models may be used to determine *vibration induced* solder strain history. SAC305 model constants for the generalized Manson-Coffin model

$$\left(\frac{\Delta \epsilon}{2}\right) = \epsilon_f \left(N_f\right)^c + \frac{\sigma_f}{E} \left(N_f\right)^b$$



have been published [25]. Vibration testing is most typically performed during product qualification using test methods described in MIL-STD-810. Test acceleration factors are often calculated using life assessment models or the Basquin relationship [26]

$$N_t S_t^b = N_u S_u^b$$

using an exponent which can range between four and nine. Qualification testing is not typically performed to failure.

- Issues/Gaps/Misconceptions

*Tests to failure* of assemblies are expected to help identify reliability issues, but MIL-STD-810 and other tests do not require *tests to failure*. Passing a qualification is insufficient to determine life expectancy.

The modeling issues presented for the temperature cycling fatigue, as stated in previous sections, also apply for predicting vibration fatigue. The level of testing and data available for model development and validation for vibration fatigue is extremely limited. Isothermal aging of solder has been demonstrated to reduce vibration fatigue life of both SnPb and mainstream Pb-free solders. However, Pb-free solder exhibits a stronger aging dependence which makes it difficult to properly evaluate the effect during vibration testing.

The majority of reported vibration test data has either been from step stress tests showing SAC soldered interconnections failing prior to SnPb joints, or from time terminated tests with no failures for mainstream Pb-free solders. The latter results do not allow for the development of fatigue models, and the use of step stress tests requires the assumption of damage accumulation models unlikely to be even roughly valid (see *Combined Loading*).

A further challenge with vibration is that the failure of traces near the solder bond pads tend to confound model development, since fatigue constants and stress states are different for the traces, than for the solder. Elevating vibration stress levels in a step stress test can transition failure from a high cycle to low cycle fatigue involving crack growth in the interfacial intermetallics. Step stress test may thus suggest a higher acceleration of damage than will occur under normal field conditions.

- Conclusions and Recommendations

Current vibration test practices in process and product validation may be sufficient to identify defects and prevent early failures. However, the lack of test to failure under single load levels, knowledge of mixed alloys, and micro-structural aging, does not allow confidence in model estimates.

Further research should be sponsored to establish vibration fatigue models based on package types and mainstream Pb-free solders used in CCA.

### *Shock Fracture and Low Mechanical Cycle*

As loading rates increase, solder interconnect failure location tends to change from solder to intermetallic bond and trace fracture due to pad cratering. Limits and trends vary with design and materials, but shock fracture and low mechanical cycle failures tend to occur by cratering (see *Pad Cratering* in Section 7.2.4, Tin Pest) or at the interfaces. This is strongly exacerbated by the combination of harder Pb-free solders, weaker intermetallic structures, copper dissolution, poorly fabricated or unqualified board materials, and the sporadic occurrence of greatly defective intermetallic structures.

- **Current Baseline Practice**

Shock and drop test standards are well established [27-31] and equally valid for Pb-free assemblies. There are currently no credible models or predictions for failures of interfacial intermetallic bonds or by cratering. At this time, the best current baseline practice is not to attempt to accelerate test conditions of shock and low cycle vibration, but rather to closely simulate actual service lifetime exposure during testing.

- **Issues/Gaps/Misconceptions**

Existing predictive models do not account for factors such as mixed alloys, aging, or competing/combined failure mechanisms. As a result, little confidence can be placed in existing models for predicting failure under shock loading conditions.

Issues with an intermetallic bond can greatly affect shock performance. Unfortunately, these defects are sporadic and therefore are often missed due to sample size limitations. Sporadic defect mechanisms are also difficult to study and proposed remedies are hard to validate (proving a negative). Problems associated with various pad finishes are commonly declared solved because they “went away.” The problem is surmised to have resulted from unspecified “process control problems” which are invariably claimed by suppliers, to be safely prevented for their products.

The gold embrittlement problem associated with excessive gold on Ni/Au pad finishes leading to a weak or less fatigue resistant intermetallic bond to the Ni, has received limited attention [32]. *Rules of thumb* for SnPb solder have not been examined sufficiently for main stream Pb-free solder alloys. Limited data suggests the problem is **reduced** for SAC solder [58]. In addition to gold embrittlement, new plating protocols and screening tests continue to be proposed and implemented to prevent black pad as phenomena also associated with Ni/Au pad finishes. Champagne voiding on immersion silver finishes appears preventable through new, published, industry practices [33]. Other defects are reported anecdotally and are often misinterpreted.

- **Sporadic Copper Nickel Tin Failure:** Occasionally, a batch of BGAs with SAC balls will arrive with one to two balls missing from each. Otherwise, a batch will show brittle failure at Nickel pads on the component substrate soon after assembly to copper pads on the PCB. This problem has been traced to the quality of the plated Nickel on the component, but is not otherwise understood.
- **Copper Pad (Kirkendall) Voiding:** The sporadic formation of voids near the interface between copper and the intermetallic bond continues to be underestimated across the industry. The problem is caused by the incorporation of impurities into the copper [59]. Pb-free solder with less ductility can exacerbate the problem. A quantitative understanding of the problematic mechanism, along with how the phenomena is accelerated, has generated some established practical remedies that still need to be implemented in a production environment [34].
- **Black Pad Fracture:** This problem is unique to Electroless Nickel Immersion Gold (ENIG). The harder Pb-free solders strongly enhance the problem.
- **Conclusions and Recommendations**  
Shock and harsh mechanical cycling is most likely to cause a solder joint to fail by pad cratering or through the intermetallic bond to a pad. Either type of failure is dominated by defects, induced in processing or subsequent handling and service.

We recommend avoiding the use of Pb-free solder attachments in field mission-critical A&D hardware for applications that are subject to long-term aging, followed by significant shock levels. Shock resistance will depend upon the nature of the intermetallic interfaces, which will be affected by long-term aging in ways that we cannot predict now. If Pb-free solder attachments must be used, we recommended that accelerated aging be performed until the intermetallic thickness matches the thickness that is anticipated after worst-case service life, prior to performing conservative lifecycle shock testing.

We recommend a systematic research effort to fill the gaps identified above.

### *Combined Loading*

Most A&D products are subjected to simultaneous and/or sequential combinations of loading while in use. As a result, tests that apply two or more concurrent loads in the hope of simulating actual field conditions are often used in product qualification. The most common combinations are the simultaneous application of temperature cycling and vibration, ESS, random vibration testing, and HALT testing. **Sequences** of different thermal excursions or mechanical loads, which are common in service, are usually not tested.

## 7. Reliability

---

- Current Baseline Practice

HALT testing is being performed on Pb-free product no differently than has been performed on SnPb products previously. HALT is intended to identify weaknesses rather than to be used for making life predictions.

Current practice for estimating life expectancy under combined loads is to apply a linear damage model that determines damage rate under individual loading conditions and sums up the damage. This can be expressed by:

$$\frac{1}{T_i} = \frac{1}{T_c} + \frac{1}{T_v}$$

Where:  $T_i$  = time to interconnect failure in that cycle,  $T_c$  = time to failure under thermal load, and  $T_v$  = time to failure under that vibration load.

- Issues/Gaps/Misconceptions

Loading (damage) history can impact the damage rate under future loading conditions. Predictions based on current industry practice of linear damage superposition may therefore be non-conservative. Attempts have been made to resolve this issue [35, 36], but a general industry consensus on a modeling approach has not even been established for SnPb. The ability to model combined loading conditions will also be strongly influenced by package formats that produce varying stress states within solder joints under combined loading conditions.

Recent work has shown an even more obvious breakdown of the linear damage assumption for sequential loading of lead free solder joints. Isothermal cycling (e.g., vibration) with a particular amplitude either **reduced** the life in subsequent cycling with a different amplitude by a factor of three more than predicted, or it **extended** subsequent life by a factor of two, depending on the combination of parameters. The potential consequences for any kind of cyclic loading are therefore significant.

- Conclusions and Recommendations

ESS testing of Pb-free solder joints may easily be much more damaging than assumed, e.g., accelerated testing should be conducted **after** screening. Predictions of life under service conditions involving varying loads or thermal excursions, not to mention simultaneous loads, may be greatly misleading. There is an urgent need for systematic materials science-based research to establish a quantitative understanding of the accumulation of damage in Pb-free solders.

Until these issues are resolved, we cannot assign a level of confidence to quantitative predictions of life under service conditions involving strongly varying loads, but errors are potentially huge.

Given the current lack of understanding, we do not recommend the use of Pb-free solder attachments in mission critical A&D products when both vibration and thermal cycling contribute a significant amount of damage.

### *Mixed Solders*

Mixing of Pb-free solder with SnPb or the mixing of two different Pb-free solders can result in solder joints that exhibit decreased reliability. Mixed alloy solder joints can pass all applicable inspections, yet may not provide a reasonable degree of reliability.

As part suppliers optimize their products for LFM&P, A&D manufacturers face a significant reduction in availability of parts with SnPb terminals. The majority of Pb-free parts with leads and leadless package formats do not pose a problem in terms of quantifying the reliability risk when assembled with SnPb solder. For Pb-free BGAs, however, assembly with SnPb solder presents a significant reliability risk [37]. The decision to combine Pb-free BGAs and a SnPb solder cannot be generally recommended, since results are highly dependent upon assembly and process. The issue of Pb-free BGAs in a SnPb solder process is covered in Section 4.0, Manufacturing. Other parts with lead (Pb) bearing terminals should not be used when changing over to LFM&P. Lead contamination has been shown to reduce Pb-free solder interconnect reliability in a highly variable fashion, and can introduce soldering defects that give rise to elevated infant mortality.

Potential mixing of disparate Pb-free solders could occur during repair activities. The effect of this on reliability is not understood and this practice should therefore be avoided. This requirement may create a significant burden during sustainment.

At present, inadequate data is available to predict the reliability for mixtures of Pb-free and SnPb solders. As such, the ***baseline practice should be to avoid mixing solders*** in assembly and rework and repair.

### *Underfill and Corner/Edge Bonding*

Due to stated weaknesses under vibration, mechanical bending, and shock, designers may seek to improve robustness of solder interconnection through underfill and/or corner and edge staking. Such applications may restrict sustainment ability by eliminating or reducing the ability to repair/rework the CCA.

- **Current Baseline Practice**  
The need for underfill and component staking may arise from prototype testing and design experience. When selecting and using underfills and compounds for component staking, it is critical to evaluate the impact of underfill through all anticipated life cycle loading conditions. For instance, it is known that underfills can shorten temperature cycle failure life of solder joints while extending vibration life times. Further, the application of underfills should be considered with respect to the assembly process and potential rework and repair operations. Rework/repair in areas adjacent underfilled parts may be also be inhibited.

## 7. Reliability

---

- Issues/Gaps/Misconceptions

The compatibility of underfills and staking materials with LFM&P needs to be understood. Poor adhesion with underfill or staking can create a larger problem.

Finite element modeling approaches for assessing life expectancy of underfilled and staked interconnect have been published. These published techniques have been demonstrated with one or more test conditions. However, the effectiveness of these modeling techniques for estimating life expectancy over long-term operation has not been satisfactorily documented. With regards to LFM&P, very little data is available.

- Conclusions and Recommendations

Different materials are preferred for Pb-free than for SnPb. Flip chip underfilling is a very mature field, and most experiences apply to WL-CSPs. Other component underfilling is far from mature. Current repairable underfills may **reduce** Pb-free performance in thermal cycling – none of them improve it significantly. If repairability is required, consider corner/edge bonding instead.

Service relevant conditions (strain rates, heating/cooling rates and maximum temperature) should be accounted for in accelerated testing if possible. Otherwise, independent materials testing should be employed to show that underfill creep can be ignored. Testing should emphasize long term degradation of underfill repairability with temperature and humidity (in the presence of realistic residues).

Non solder mask defined pads on PCB should be designed to prevent air bubble entrapment.

### *Low Temperature Brittle Fracture*

In contrast with SnPb, SAC solders have exhibited a rapid transition from ductile to brittle fracture between -40°C and -70°C [38]. For A&D applications operating at extremely low temperatures, particularly under high stress and high strain loading conditions such as in mechanical shock, this may present a risk.

- Current Baseline Practice

MIL-STD-810 requires testing at the minimum temperature if service extends into the brittle fracture regime, but this is not always rigorously followed.

- Issues/Gaps/Misconceptions

Little information is available about SnPb solder behavior under shock and vibration at low temperatures, but many decades of successful field history in A&D products provides empirical assurance. No such assurance currently exists for Pb-free solders.

Existing models for shock do not adequately consider impact of the low temperature transition on solder properties. Current test practices may ignore low temperature effects, resulting in unexpected failures with Pb-free materials.

- Conclusions and Recommendations

For applications involving mechanical shock below  $-40^{\circ}\text{C}$ , mechanical testing should be performed at or below in-use temperature. Indications are that a problem may exist but further research is required to develop constitutive and failure models so rules of thumb can be established.

## 7.2.2 Creep Rupture

Creep rupture occurs when a solder joint continues to yield under a sustained load until it can no longer support the load, leading to catastrophic failure. For example, a manifestation of a sustained load can be exerted by wires under tension. CCAs are often subjected to a constant bending load due to fixturing in housing or a shear load if mounted vertically with heavy components. Aging of the solder will affect the creep behavior of the solder, and as a consequence, isothermal aging may strongly reduce the ductility of SAC solders and accelerate creep rupture (Figure 7.5).

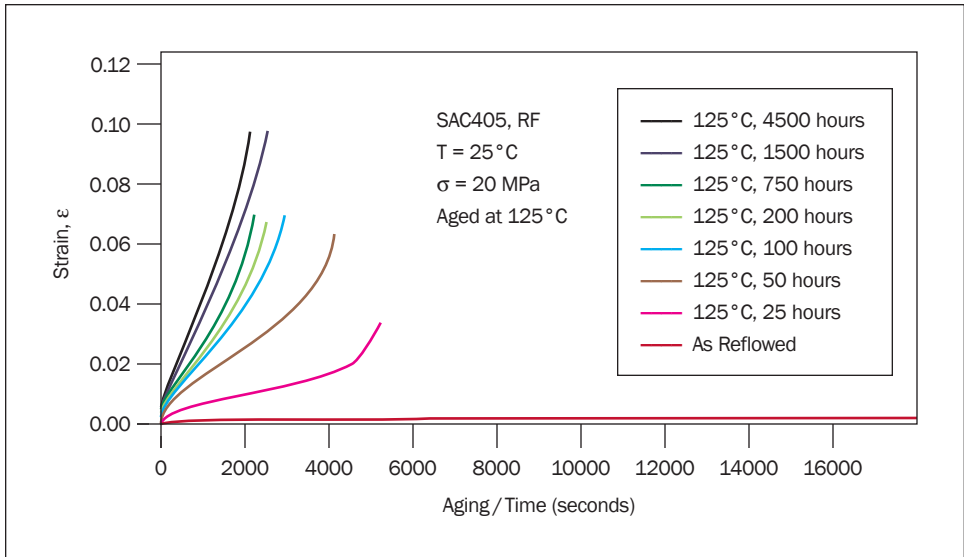


Figure 7.5 Creep curve for SAC405 after select isothermal aging conditions [39].

## 7. Reliability

---

- **Current Baseline Practice**

Existing design practice aims to eliminate steady-state stresses on solder joints. However, variations in manufacture and assembly can result in the presence of steady-state stresses and the risk of creep rupture.

Testing for creep rupture is not normally performed at the CCA level, but it is identified in industry standards such as IPC-SM-785. As with SnPb, the creep behavior of Pb-free solders exhibit primary, secondary, and tertiary zones. The primary zone is more pronounced for Pb-free and may be modeled by a generalized exponential model. The secondary zone may be modeled with a Garofalo Hyperbolic Sine Model. Despite a significant amount of research, failure models for assessing creep rupture in solder interconnects are not readily available.

- **Issues/Gaps/Misconceptions**

Effects of Sn grain orientation may lead to significant scatter in creep properties [4], an effect that is likely to vary significantly with solder joint size.

It is a misconception that mainstream SAC solders always creep less than SnPb solder. Creep is highly dependent upon stress level, temperature, and isothermal aging state.

- **Conclusions and Recommendations**

For applications involving a sustained load on the interconnect, creep rupture presents a reliability risk. This is particularly true for aged low silver content SAC solders.

Do not use SAC solders with less than three weight percent silver in applications where creep rupture may be a failure source.

Acceleration factors for creep rupture onset must be established between test and in-use condition over the lifetime of the product.

### 7.2.3 Electromigration

For SnPb solders, electromigration tends to become significant at direct current densities and above  $10^4 \text{ A/cm}^2$ , so it is primarily considered a risk for high power flip chip applications. Current practice is to control current densities below  $10^4 \text{ A/cm}^2$ . The same accelerated test practices and models that were used for SnPb continue to be used for Pb-free.

Accelerated testing suggests that the problem may not be significantly worse with Pb-free solders, and that the legacy models and tests are still applicable. It is common to focus solely on failure by electromigration, ignoring interactions with aging and effects on life under loading conditions such as temperature cycling, vibration, and shock. A redistribution of intermetallic precipitates may have



serious consequences regarding material behavior. There is anecdotal evidence that relatively low levels of electromigration can affect the thermal fatigue resistance of Pb-free solders and accelerate Kirkendall voiding in intermetallic bonds to copper pads.

We recommend systematic research to characterize the effect of electromigration on thermal fatigue resistance of Pb-free solders and to develop quantitative models.

In the absence of life time data or validated models, we recommend against use of direct currents above  $10^3 \text{ A/cm}^2$  in Pb-free solder joints.

### **7.2.4 Tin Pest**

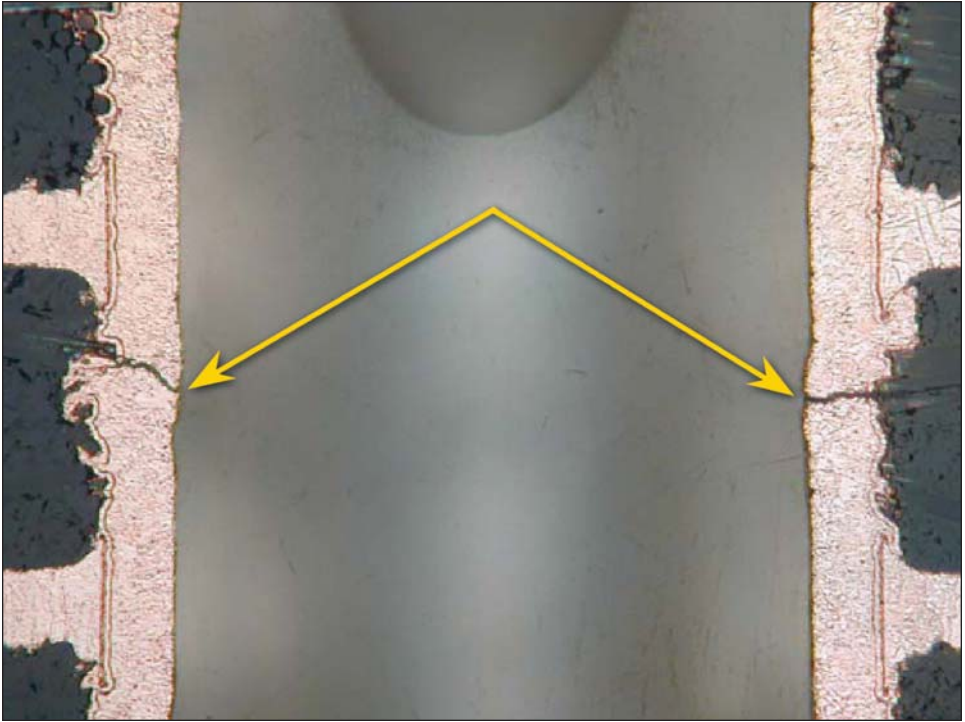
Metallic tin is susceptible to transformation to a nonmetallic form when exposed to cold temperatures for extended periods of time, leading the tin to crumble into a nonconductive dust. This phenomenon is known as “tin pest.” The incorporation of lead into tin is known to suppress this transformation. To date, tin pest has not been shown to occur in Pb-free solder assemblies. This includes temperature cycling conditions with minimum temperature at or below zero. It has been postulated that a rise above the transition temperature ( $13^\circ\text{C}$ ) may reset the time to conversion, but two years of sub-zero storage of SAC soldered assemblies [40] or four years of low temperature storage [41] did not lead to tin pest either. Still, whether or not actual Pb-free solder joints may be susceptible to it during extended cold service remains unknown [42].

Susceptibility to tin pest may well vary with Pb-free composition, including the presence or absence of particular low-level contaminants picked up during assembly. This significantly complicates the generation and interpretation of tests.

Until such time as the risk can be properly defined, it is recommended that Pb-free solder joints not be used in high reliability A&D assemblies, which will be completely inaccessible for repair and that are anticipated to be continuously exposed to temperatures below  $0^\circ\text{C}$  for extended periods of time (greater than two years).

#### *Barrel Cracks*

Copper metallization in PCB plated-through holes is subjected to mechanical damage due to assembly, rework, and repair operations. Further damage can occur under temperature excursions in screening and use. Accumulated mechanical damage can result in loss of electrical continuity due to complete barrel cracking. Such failures are strongly influenced by the quality of the board fabrication process as well as the life cycle loading conditions. Higher Pb-free process temperatures alone will increase damage levels in PTH interconnects. This damage can lead to reduced ability to rework/repair assemblies and result in earlier than expected wearout. Models have been developed to predict barrel cracking [43]. High aspect ratio PTHs present the highest risk [44].



**Figure 7.6 Barrel Cracking**

- **Current Baseline Practice**  
Interconnect Stress Testing (IST) is widely used for verifying that PCBs can survive multiple reflow operations and provide sufficient service life.
- **Issues/Gaps/Misconceptions**  
Barrel fatigue models have been established for SnPb assemblies. It is unclear if the models need to be updated based on the stress levels that can occur in a Pb-free soldering operation.  
  
The ability to repair CCAs may be limited with Pb-free solders due to higher damage sustained under elevated Pb-free soldering operations.
- **Conclusions and Recommendations**  
Increased temperature in assembly and rework can lead to damage of plating in PTHs resulting in elevated infant mortality and early life failures.

Current practice of using IST should be applied in qualifying board fabricators. This practice should eliminate early failures. Onset of wearout should be assessed in light of damage associated with the higher Pb-free soldering operations. Before such testing, we recommend pre-conditioning the PCB in multiple Pb-free reflows.

Printed wiring boards must be qualified for temperatures encountered in Pb-free assembly process.

### *Trace Fatigue Cracks*

High cycle mechanical loads can lead to trace cracking because of poor adhesion between the copper and laminate, in high stress concentrations where the trace escapes the solder mask, and in cratering of the underlying resin (see *Pad Cratering*). Trace crack failures have not generally been associated with in-use product failures, but the adoption of Pb-free solders may change this.

- **Current Baseline Practice**  
Trace cracks have not been a major issue with SnPb solder. Material testing may be done periodically by board fabricators and some equipment manufacturers, but it is unclear that sufficient attention has been paid to trace fracture. Test methods for copper ductility and tensile strength are available in IPC-TM-650.
- **Issues/Gaps/Misconceptions**  
The high moduli and propensity for copper dissolution of mainstream Pb-free solders may increase the likelihood of trace cracking, but failures are often conflated with other failure modes induced by mechanical shock and vibration.

Models for assessing trace cracking are not readily available. As a result, critical material properties of copper and copper to laminate adhesion have not been identified.

- **Conclusions and Recommendations**  
With the conversion to mainstream SAC solders, trace cracking may result in earlier than expected wearout failures and random failures due to uncontrolled copper dissolution and pad cratering. Control parameters have not been established.

Better evaluation methods and guidelines are needed to reduce probability of failure due to trace cracking.

### *Pad Cratering*

Pad cratering is described and illustrated in Section 4.0, Manufacturing.

## 7. Reliability

---

- Current Baseline Practice

Cratering may be considered a component substrate as well as a PCB defect. Efforts are ongoing to define a new IPC standard for joint level testing to replace CCA testing for cratering under a single overstress or shock. At present, no credible models are available for the prediction or extrapolation of joint or CCA level test results.

- Issues/Gaps/Misconceptions

Trace failure due to cratering competes with solder and intermetallic failures, but it is sensitive to very different factors. Cratering will also influence time to solder or intermetallic failure. This greatly complicates the generalization and extrapolation of CCA level test results to service conditions.

A common misconception is that test results can be generalized more than is warranted. Attempts at interpretation rarely distinguish failure under an overstress or shock from wear out under repeated loads (vibration, drops). However, mechanisms and systematic trends are completely different. Notably, repeated loading is much more sensitive to defects. Also, effects of different degradation mechanisms vary with design.

Rework reduces the resistance to cratering in subsequent cycling. However, repair is of much greater concern because the preceding aging and humidity exposure further reduces the resistance to the initiation of defects.

- Conclusions and Recommendations

An unavoidable consequence of repair is a significantly reduced resistance to cratering in subsequent vibration or, potentially, even thermal cycling.

It is recommended that further systematic studies be performed to support development of a standard for joint level testing of cratering under overstress.

A combination of joint level and CCA level testing should be used to qualify rework and repair processes. Evaluation of qualification samples should include cross-sectioning to check for evidence of incipient cratering.

### *Conductive Anodic Filament Resistance Drops*

CAFs are copper corrosion byproducts growing from the anode towards the cathode of a circuit below the surface of a PCB, commonly along separated fiber-epoxy interfaces [44, 45]. Studies by CALCE, University of Toronto, Unovis and NPL have demonstrated that board test specimens subjected to elevated Pb-free process temperatures have a higher propensity to CAF failure.

Standard CAF test procedures for SnPb still apply where specially designed test coupons are required. For board qualification, test procedures must address the impact of Pb-free reflow and wave solder operations as a precondition to any CAF tests. PCB suppliers do not usually test for

effects of defects created in assembly or use. Such defects are much more prevalent for Pb-free solders and compatible laminates [46]. A particular concern is defect generation in repair.

Tight conductor spacing, high voltage potentials, and high moisture uptake tend to aggravate increase CAF failures. Introduction of new laminate materials and changes in materials will require strict surveillance of CAF performance.

### *Creep Corrosion and Dendritic Growth*

An important function of the printed wiring board is to provide high surface insulation resistances between adjacent metal conductors of separate electrical circuits. Moisture in the presence of mobile metal ions can result in a loss of surface insulation and ultimately electrical failures. Unlike interconnect failures, surface insulation failure can occur randomly and may be tied to materials selected in design as well as processes used in manufacturing. Corrosion and dendritic induced failures have been held at a relatively low level due to cleaning processes, elimination of active ions in reflow, selection of metal finishes, solder mask materials, and fabrication processes that greatly reduce the risk. Pb-free materials and processes introduce an increased risk for creep corrosion and dendritic failures which occur and evade product validation tests. A clear example is the creep corrosion failures on immersion silver finished CCAs used in computer applications that occurred in sulfur rich environments (Figure 7.6) [47].

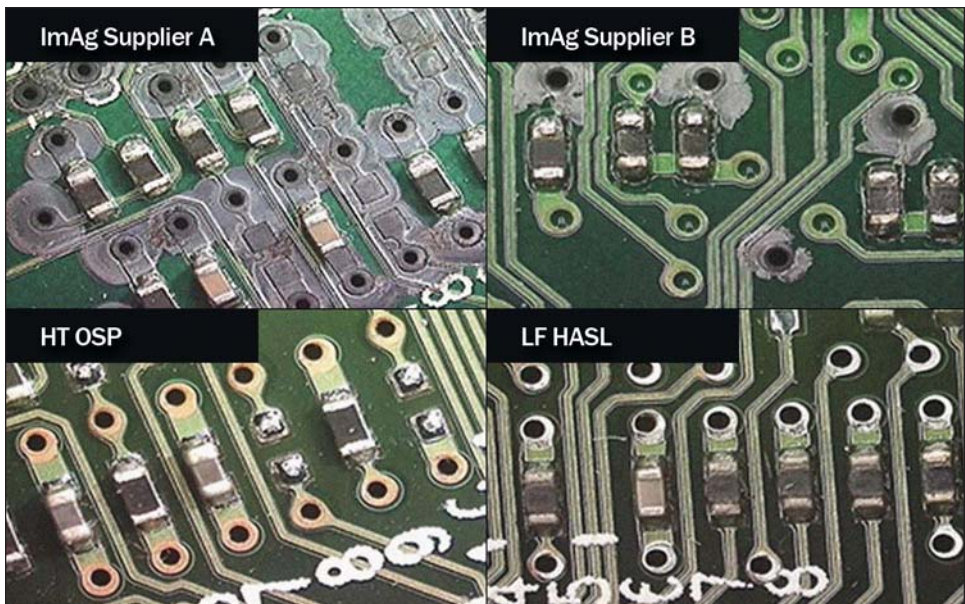


Figure 7.6 Comparison of board finishes under sulfur rich environments.

## 7. Reliability

---

- **Current Baseline Practice**

To identify surface electrochemical migration issues, board fabricators and CCA manufacturers use tests set forth in IPC-TM-650. These tests include SIR and electrochemical migration. Mixed flowing gas (MFG) tests are also used to examine the propensity for surface corrosion.

- **Issues/Gaps/Misconceptions**

Despite testing, creep corrosion failures escaped the Pb-free product development process and caused significant financial losses. This indicates a deficiency in existing test methods to help scrutinize products that can potentially fail due to creep corrosion and dendritic growth.

New processes and materials can produce unexpected failures that will increase early and useful life failures. Rapid adoption of new processes and material by A&D industry could result in severe consequences. Current qualification test methods have been shown to be insufficient in preventing electrochemical induced failures.

Poor wetting of Pb-free solders and higher surface damage, induced by reworking Pb-free assemblies, may result in exposing the copper pads or traces to environments which could lead to electrochemical induced failures.

- **Conclusions and Recommendations**

New test methods are needed to qualify PCB finishes that prevent electrochemical migration failures.

Immersion silver PCB finishes should not be used in A&D products, unless adequate protection against airborne or material induced impurities which promote silver oxidation or chemical corrosion has been provided, and validated by test.

### 7.2.5 Tin Whisker Shorting

Tin whiskers can grow spontaneously from tin rich surface finishes, reaching lengths ranging from a few microns to several millimeters. Their diameters typically range from less than a micron to about 10 microns, making them very difficult to see even under optical instruments. Whiskers are electrically conductive, presenting risks of electrical shorting and arcing failures. Historically, tin whiskers have been associated with catastrophic system-level failures in A&D hardware [48]. The removal of Pb, a recognized mitigator of tin whiskers, has raised serious concerns over the inclusion of Pb-free parts in A&D systems.

Tin whisker incubation periods can range from days to years, and lengths have been shown to follow a lognormal distribution [49]. As such, it is not clear from statistical assessments, that growth is ever completely arrested. Current industry consensus is [50] that the fundamental mechanisms of whisker growth are too insufficiently understood to predict whisker growth for long periods. Tin whiskers can escape detection during initial screening and testing, only to show up in the field,

where there is generally no accepted minimum or maximum time in which tin whisker growth has been declaratively terminated, and can be regarded as innocuous. For most A&D systems, tin whisker induced unreliability will result from randomly distributed failures that manifest themselves as a decreased MTBF at the system-level. Most of these failures will be intermittent, and extremely difficult to properly troubleshoot.

- **Current Baseline Practice**

The preferred baseline practice is to implement tin whisker risk mitigation plans in accordance with GEIA-STD-0005-2. This document discusses various mitigation activities to be implemented throughout all phases of a program. Details provided in this document and its appendices will not be repeated here.

During the design phase, it is necessary to specify mitigation strategies and techniques. This leads to a decision process whereby the adequacy of the mitigations needs to be assessed. Two published models currently employed in the A&D community can be used for this purpose, the so-called “Pinsky model,” and the CALCE “tin whisker risk calculator” [51, 52].

Component level testing intended to evaluate whiskering propensity is described in the commercial standard JESD-201. This standard includes in its introduction, a statement to the effect that Pb-free tin should not be used in Class 3 products, which includes A&D.

From an A&D equipment manufacturing perspective, three options exist: application of conformal coating, replacement of the tin by SnPb by solder dipping or special plating processes, and reliance on SnPb solder wicking in the assembly process to completely coat Pb-free tin surfaces. Each approach has positive and negatives which need to be considered in the design and manufacturing phases. Qualification of one solder dipping process was provided by a Navy funded project [53]. An industry standard, GEIA-STD-0006 has been issued to cover qualification of these solder dip processes.

- **Issues/Gaps/Misconceptions**

Conversion to Pb-free electronics systems does not mitigate the tin whisker risk.

Fundamental physical models describing tin whisker growth have not been fully developed nor widely accepted. As a result, the available models cannot be used to accurately quantify the risk associated with tin whiskers.

Conformal coating provides a high degree of mitigation. However, no coating is perfect and tests indicate that nearly all commonly used coatings can be penetrated by whisker growth. Furthermore, the long-term effectiveness of conformal coating as a whisker mitigator has not been quantified.

The diligence required to prevent an unacceptable incorporation of tin adds cost and often results in schedule slippage during manufacture.



## 7. Reliability

---

The tin whisker phenomenon is subject to a number of misconceptions including:

- Tin whisker failures can only occur in space-based systems (untrue).
  - Tin whisker growth requires the presence of voltage (untrue).
  - Tin whisker growth only occurs in harsh environments (untrue).
  - For a given finish, there is a maximum length beyond which whiskers cannot grow (untrue).
  - If there's sufficient voltage to fuse a whisker open, failure cannot result (untrue).
- **Conclusions and Recommendations**

The incorporation of pure tin finishes into A&D systems is a present reality. Present management of tin whisker risks is not optimal, resulting in undefined reliability risks for fielded systems and unnecessary cost and schedule impacts to A&D programs.

Tin whisker risks should be managed using GEIA-STD-0005-2.

Investigations into currently applied mitigation techniques should be performed with a goal to quantify their efficacy. Development of improved mitigation techniques should then be undertaken, with the goal to developing more effective techniques where necessary.

Development of a meaningful test to predict tin whiskering propensity for components should be undertaken.

Additional research should be performed to provide greater basic understanding of the tin whiskering phenomenon.

### 7.2.6 Parts (Not PCB)

#### *Temperature Sensitivity*

Mainstream Pb-free solders require process temperatures that can be 20 to 40 °C higher than SnPb solder. While the part supply chain has rapidly converted to Pb-free terminal finishes, many part types still have temperature limits that make them susceptible to damage in a Pb-free assembly process. J-STD-075 has recently been issued to provide a standard for qualifying and identifying temperature sensitive parts.

#### *BGA CTE Warpage*

BGA to PCB co-planarity is essential for forming quality interconnects. BGA packages can warp at elevated temperatures, which is exacerbated by the increased Pb-free processing temperatures. JESD-22-B112 has been established as a test to quantify warpage. Warpage issues are normally found in production and may be considered a form of temperature sensitivity.



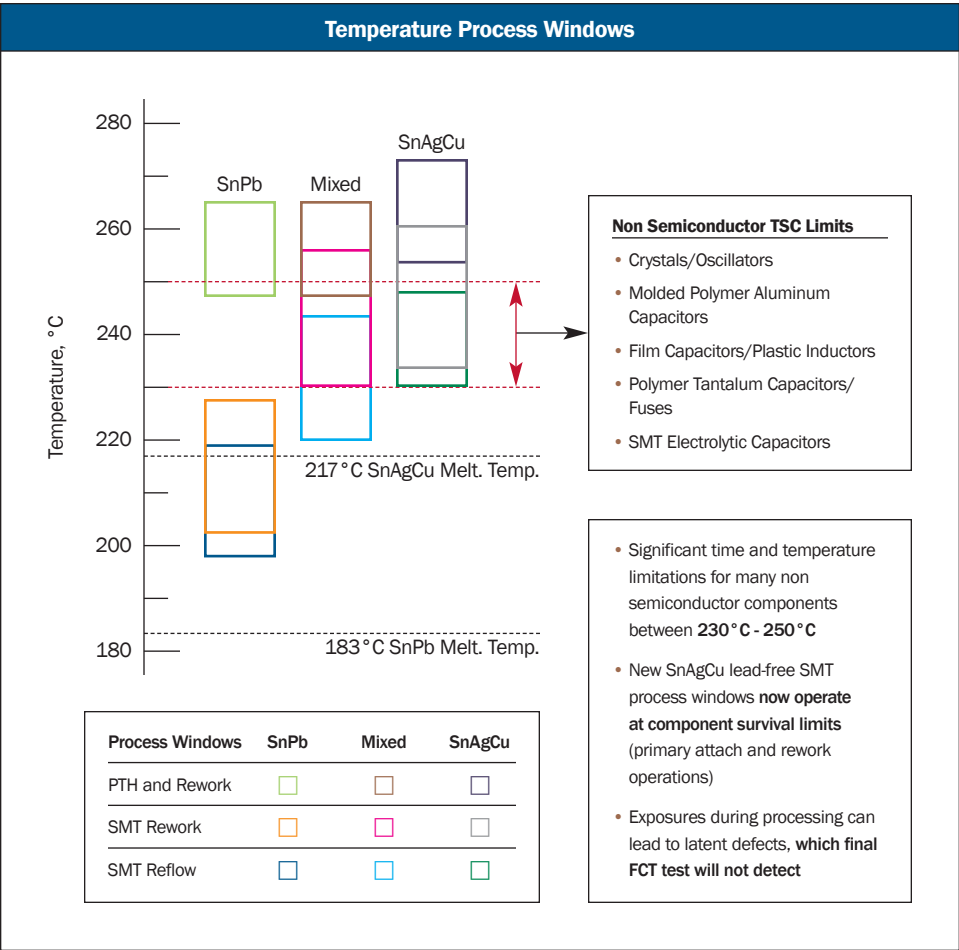


Figure 7.7 Temperature Process Window, courtesy of IBM Corporation.

- Recommendations  
The provisions of J-STD-075 should be employed to manage the effects of temperature sensitive parts on assemblies.

The provisions of JESD-22-B112 should be employed to measure BGA warpage. An industry consensus should be arrived at regarding acceptable levels of BGA warpage.

“Computing machines perhaps can do the work of a dozen ordinary men,  
but there is no machine that can do the work of one extraordinary man.”

—E. B. White (1899-1985)



photo courtesy of dix

# 8. Conclusions

## 8.1 OVERVIEW

The Phase I Manhattan Project Team has collectively documented a set of baseline best practices for addressing risks associated with the use of Pb-free, within the context of a product life cycle model. Drawing upon this collective body of expertise and knowledge, the following sections provide a summary of the major conclusions documented within the body of this report.

The effect of introducing Pb-free materials in A&D applications presents potential risk issues. An appropriate amount of scrutiny and resources should be utilized to address the surplus of unknown performance and reliability of Pb-free material. The problem is real and may manifest itself from the innocuous to the catastrophic.

The efforts of the Lead Free Electronics Manhattan Project – Phase I have shed considerable light onto the uncertainties regarding the consequences of utilizing Pb-free materials, intentionally or otherwise, in A&D programs. The various electronic material suppliers are not aware, or have little control over the supply chain and cannot prevent the admission of Pb-free products into the manufacturing flow. The challenge in mitigating the entry and effects of Pb-free materials is uniformly distributed across the product life cycle.

The best current baseline practices, outlined in this report, are to be considered a foundation for the subsequent research which will be used to solidify the gaps in Pb-free electronics. What can be validated through experimentation and data collection, must be part of a collective and comprehensive effort on the part of industry, DoD, consortiums and academia. The risk of a fragmented effort will only lead to both the replication and omission of critical projects, at a much higher cost, and more importantly, a remission in finding plausible solutions.

## 8.2 DESIGN

The process of managing Pb-free risk begins in the early stages of an assembly or CCA design, where a greater impact can be made toward controlling and mitigating effects. Based on the findings of the Phase I Manhattan Project Team SMEs in the field of design, the following conclusions were drawn.

- The implementation of a Lead Free Control Plan is a necessity.
- Designers must be acutely aware that there are no heritage products from which to derive design rules.
- Single drop-in replacements do not currently exist that will conform to present SnPb baselines.

## 8. Conclusions

---

- Established practices and analytical techniques such as FMEA can be used, but with extreme caution. Modifications to these tools will need to be made to help improve detection of intermittent electrical failures.
- An accurate accounting of the environmental conditions is required for Pb-free.
- There is a critical need for controlled documentation, verification and selection process for the construction of a BOM.
- More stringent procedures need to be implemented for product qualification due to latent damage to PCBs subjected to Pb-free processes. This may require a larger sample of qualification lots.
- Designing to mitigate the effects of vibration will be paramount in Pb-free systems. The placement location of key components and stabilizing structures onto the assemblies may be needed.
- Computational models are needed to develop test parameters for Pb-free.
- The designer should expect that new failure modes will occur with Pb-free.

### 8.3 MANUFACTURING

The manufacturing process plays a fundamental role in developing the structure and morphology of solder joints, which will eventually form into an interconnection. The manufacturing processes for Pb-free are at a greater maturity level than the other supporting sectors of electronic assembly production, but face difficult challenges nevertheless. Engineering changes to the manufacturing process will be necessary for adaptation to Pb-free materials, since a mixed material set of SnPb and Pb-free will need modified process parameters to form a proper solder joint. Faced with these prospects, the manufacturing experts conclude:

- The use of Design for Manufacturing (DFM) tools are critical in establishing processes and procedures that will guard against the potential consequences during the Pb-free transition. It is of paramount importance that first article inspections are adhered to with close scrutiny of the results.
- Some amount of process development will be needed to optimize manufacturing for Pb-free materials. There are no existing “drop-in” processes.
- Plan for the need to modify equipment capability. This is particularly true for reflow ovens, wave solder, and hand soldering tools.

- The Pb-free solder will behave differently and will look different. Because of this, training of operators and other personnel will become crucial.

### 8.4 SUSTAINMENT

The reduced availability and increased cost of SnPb parts has made the task of sustainment more difficult, and has had a profound effect on all the elements of logistics management. Everything from configuration control, design traceability, part replacements, and material compositions has been affected by the transition of the COTS electronic industry from SnPb to Pb-free. A common conclusion that appears throughout the entire report is the failure of suppliers to document when changes have occurred; assuming the posture that small changes in material composition (e.g., component finish) do not violate the fit, form, and function directive for initiating an Engineering Change Notice (ECN). This conclusion is relevant to all areas, including sustainment, where traceability of original assemblies and materials is crucial to the rework process. The sustainment experts concur that:

- There needs to be a sustainable effort to ensure that data and information regarding any constituent part or material that goes into the construction of the electronic assemblies is known, adequately documented, and properly communicated through the product life cycle.
- There should be a flow of communication between the repair process group, logistics, and configuration management to ensure that repair documentation is updated, materials for assembly repair are defined, and part replacements are made available.
- Training of depot repair and other related sustainment personnel on Pb-Free will be required.

### 8.5 TESTING

The failure to document changes to the material composition from SnPb to Pb-free creates a risk when assessing the reliability of the assemblies. ESS and other testing procedures have been structured to provide the most accurate characterization of SnPb in actual field conditions. The test conditions simulate the long term field effects that have not been defined for Pb-free materials, thereby creating an uncertainty in the accuracy of the results in predicting failure when using SnPb test conditions. The team has concluded the following:

- Though equipment presently exists to adequately test for Pb-free assemblies, test conditions and protocols have not yet been defined to provide adequate computational models to simulate service lifetime conditions.
- Current test methods are not adequate for Pb-free A&D electronic assemblies.

## 8. Conclusions

---

### 8.6 RELIABILITY

Analysis of the reliability of Pb-free electronic assemblies has shown a consistent theme, asserting that the use of SnPb constitutive and predicative models cannot behave as adequate substitutes for characterizing Pb-free material behaviors. Essentially, the characteristic material properties of Pb-free are sufficiently different from SnPb, as to invalidate any assumptions predicated on the hypothesis. This is the case when subjecting both materials to thermo-mechanical stress or shock – the reliability results are unchanged. There are a number of factors which are integral in providing a validated model to predict lifetime behavior of a solder joint; unfortunately, at the present time, there is insufficient information about Pb-free solders to make a reasonable lifetime prediction. The reliability team concludes:

- Data to support reliability models for Pb-free is insufficient to make predictions on the long-term behavior of Pb-free assemblies for A&D programs.
- Pb-free materials are more susceptible to mechanical shock and vibration than SnPb.
- Thermo-mechanical behavior of Pb-free materials at varying temperatures is different than that of SnPb, especially at the low temperature extremities. This is a major concern for A&D products.
- There may be a need for certain pre-conditioning steps prior to ESS to properly assess the effect of the respective environmental test.
- There is no exacting method of mitigating tin whiskers at the present, other than to avoid pure tin.

### 8.7 TIN WHISKERS

Pb-free solder joint reliability is one major concern for the electronics industry, especially in A&D applications; the risk associated with tin whiskers is equally serious. Tin whiskers continue to be a source of consternation for high reliability product providers. The history and the subsequent effects of tin whisker growth have been well known in an anecdotal manner over a number of years. The list of documented failures due to the discovery of tin whiskers continues to grow as the cause of catastrophic failures in avionic and high level infrastructure systems, while many failures due to whiskers go unreported due to liability concerns. The importance of the problem has not gone unnoticed, but in recent years has been highlighted due to the Pb-free transition.

A partial list of costly electronic equipment losses and availability losses is highlighted here to underscore the serious risk associated with this phenomenon.

- Nuclear Utilities Unplanned Shutdown – availability loss
- Space Shuttle Fleet Main Engine Gimbal Avionics – availability loss
- Seven Satellites: complete microprocessor failures – hardware loss
- Patriot Missiles – availability loss
- Six Other Missile Programs: complete failure – hardware loss
- Heart Pacemakers: complete failure – hardware loss
- Heart Defibrillators: complete failure – hardware loss
- F-15 Radar – availability loss
- Several Other Military Planes – availability loss
- Telecom Equipment – availability loss

There is a myriad of activity that centers on resolving the issues of tin whiskers, from predicting their cause to growth, to mitigating the effects. Not one organizational body has the resources to address the underlying solutions to the problem on their own, while the quality of information to resolve the issue of tin whiskers is varied and contradictory. As a result, an “each man for his own good” approach has been an obstruction to discovering universally feasible solutions.

## 8.8 UNIVERSAL GAPS

The subject matter experts on the team recommend that a more inclusive, thorough research and development roadmap be developed and implemented. Generally acknowledged areas where gaps exist on a universal scale are:

1. Commercial vs. Military

The effects of product reliability and sustainment due to Pb-free electronics usage are *not* well understood. Additional empirical evidence on Pb-free electronics, especially long term reliability of greater than ten years, is needed. While some commercial telecommunications products specify lifetimes of ten years, typical A&D products such as military aircraft and missile weapon systems require much longer lifetimes, often measured in decades.

## 8. Conclusions

---

### 2. Technical Knowledge

There have been numerous Pb-free electronics research publications by the various consortia, industry and academia, representing a wide array of technical capacities. While these add a significant contribution to the overall Pb-free electronics knowledge base, it is still very limited, sparse, and often disconnected when addressing the reliability requirements of the DoD and A&D applications.

### 3. Field Failures

Field failure information regarding Pb-free electronics assemblies at this juncture is very sporadic. Equally critical, and found to be missing, is the information on the root causes in identifying mechanisms which are responsible for failure when it occurs, or how to mitigate them.

### 4. Process Control

Data to assess reliability of one specific Pb-free electronics manufacturing process over others can be difficult to interpret since many of the manufacturing variables are not consistent from one process to another. The Lead Free Electronics Manhattan Project has identified the best manufacturing current baseline practices that mitigate the effects of Pb-free electronics. However, more work needs to be done to address the various manufacturing technology gaps in order to produce greater process efficiency and controls. Manufacturing research and development will be required to reduce cost and increase the assurances of reliability control for A&D applications.

### 5. Reliability Models

There is a major shortcoming in the validation of existing Pb-free electronics reliability models to predict potential field failure and product lifetimes. The objective for Phase II of the Lead Free Electronics Manhattan Project is to develop a roadmap that integrates and prioritizes the research needed to properly evaluate the lifetime reliability modeling of Pb-free electronic assemblies.



“The secrets of nature reveal themselves more readily  
under the vexation of art than when they go their own way.”

—*Sir Francis Bacon (1561-1626)*



photo courtesy of Jenny Rollo

# 9. Recommendations

## 9.1 OVERVIEW

This report documents the current baseline practices for Pb-Free electronics mitigations and usage along with corresponding technology and manufacturing gaps. Based upon this compilation of information, the following summary recommendations are provided for the purpose of minimizing risks associated with the use of Pb-free electronics in A&D products. Additional details are contained in the appropriate sections within this report.

## 9.2 GENERAL DESIGN RECOMMENDATIONS

- As part of a risk management strategy, employ and use a structured Pb-free control plan, incorporating the existing GEIA documents as a guideline, updating where necessary for new materials and processes. See specific section on design for further details.
- Develop a Pb-free material compatibility guideline that incorporates all facets of the material selection process, which will include specifications and recommendations for design on the basis of environmental requirements.
- Product designers should consider the complications incurred by the increased mitigation efforts to reduce whiskers, as well as increased incidences of electrical failures incurred by higher manufacturing process temperatures. Also as a result of this, increase the frequency and number of both “on-board” analysis and subsequent field inspections.
- Insist that the environmental conditions be defined clearly. No cognitive design recommendations for Pb-free electronics can be made without this information. This will also affect the type and severity of the test conditions for ESS where the qualification parameters are defined.
- Expand on the criteria and data needed for a preferred parts list where necessary, and define the conditions under which a Pb-free electronic part can be added to a BOM.

- Design rules should include a strategy to handle modification of the way printed wiring boards are designed, subsequently assembled, and will include a selection of alloys and substrates potentially more suitable than what presently exists. Specialized designs for RF should also be considered. Some of the key areas:
  - Attachment Alloys
  - Component Finishes
  - Printed Wiring Boards
  - PCB Finishes
  - Mechanical Parts
- Make provisions in the design of electronic systems for field repairs, which will inevitably be subject to different soldering materials and conditions.
- An effective and rapid method of validating new designs needs to be developed which utilizes test parameters derived for Pb-free materials and conditions, and includes a variety of accelerated stress tests.
- Include tin whisker risk as part of the design criteria. Use the GEIA standards as guidelines.

### 9.3 GENERAL MANUFACTURING RECOMMENDATIONS

- Provide a comprehensive DFM plan which includes assessing all the potential processes, materials, and in-testing modifications that will be required for the introduction of Pb-free material into the manufacturing stream. Include an emphasis on first article inspection as a critical event before proceeding to manufacturing.
- Investments will have to be made to update equipment . This includes reflow process equipment, in-process inspection, and analytical equipment. Additional investments will be needed in the area of training, which includes personnel from all the areas of manufacturing.
- It is inevitable that engineering time will have to be invested to determine the parametric process window for Pb-free electronics, with an emphasis on optimizing around reflow conditions and cleaning cycles.
- Rework processes must be re-qualified with careful consideration to the additional thermal energy that will be used as part of the processes.

### 9.4 GENERAL SUSTAINMENT RECOMMENDATIONS

- Sustainment involves a large number of interactive areas, all with issues regarding Pb-free electronics. An infrastructure presently exists to accommodate the various elements of the sustainment process, but a greater concerted effort will be needed to ensure that the details – often missing for accurate management of configuration control – are available for Pb-free electronics. The particulars for the proper course of action should be decided upon collaboratively among sustainment, manufacturing, design, and the customer. The specifics should include:
  - A Lead Free Control Plan
  - Repair Procedures and Metrics
  - Pb-Free Assessment Plan
  - Feedback from the Field
  - Contingency Plan for Unavailable Parts
  - Inventory Plan to Maintain Overage
  - An Assessment of COTS as a Suitable Replacement for Repairs
- There will be heavy pressure upon repair depots to sustain Pb-free materials sets beyond their capability to handle them. It is highly recommended that repair facilities restrict their material usage to one or two selected Pb-free solders, and more critically, that the original repair requirements be modified to reflect the change.
- The original designer of the assembly must be notified of repair modifications, which may have been necessitated by an unexpected change in SnPb component or material availability. Communication between the repair depot and the original assembly designers is critical.

### 9.5 GENERAL TESTING RECOMMENDATIONS

- The upper and lower boundaries of many of the thermal cycling tests are not adequate to simulate field failures, and must be established. The same can be said for isothermal conditions for long term aging or as a prerequisite for further thermal stress testing.
- Parameters for mechanical testing (e.g., vibration) need modification; appropriate test parameters must be defined.
- Validated computational models to predict fatigue field failure must be developed. This requires detailed information on test vehicle design, test parameters, and field results.
- The JEDEC standards can be used as a guideline in the interim, but they are insufficient as an acceptance document for A&D applications.

### 9.6 GENERAL RELIABILITY RECOMMENDATIONS

- Investment in further research and characterization of Pb-free materials is needed to prevent the reliability uncertainties due to the disparity between the existing SnPb knowledge base and the more limited Pb-free electronics data pool.
- Avoid using Pb-free attachments in mission critical A&D applications.
- Research is needed on the accumulative damage to Pb-free electronic assemblies from environmental conditions under varying loads. Essentially, there is non-linear degradation that is occurring which is not accounted for in present ESS models.
- The low temperature damage ( $-40^{\circ}\text{C}$ ) to Pb-free assemblies is an issue. Constitutive models will have to be developed.
- For applications where assemblies are subjected to sustained loads, SAC alloys with <3% silver are not recommended.

### 9.7 SUMMARY OF RECOMMENDATIONS FOR PHASE II OF THE LEAD FREE ELECTRONICS MANHATTAN PROJECT

**Using the corporate knowledge collected in the Phase I deliverable, develop a research and development roadmap for future projects.**

This requires a thorough vetting of where the gaps are and how they interact with each other. For example, selection of a particular material set based on the current baseline practices may produce acceptable first tier results, but it may impact other areas that are not readily obvious. For example, selecting SAC305 solder is the commercial “alloy of choice” as a best manufacturing practice. Through a gap analysis for A&D applications, the likelihood exists that at some strain value, the composition of SAC305 may not be suitable for high mechanical stress applications. Therefore, further work on strain point limitations would be needed, precipitating a recommendation that SAC305 may not be the A&D alloy of choice under high strain conditions.

**Develop statements of work and budget estimates for the research and development projects.**

Each specific area of focus (Design, Materials, Manufacturing, Sustainment, Testing, and Reliability) has tangible deficiencies. Statements of work for projects will need to be developed, estimated, and implemented to address these deficiencies.

## 9. Recommendations

---

---

### **Document results in a “Pb-Free Electronics Risk Mitigation Research Plan.”**

Once the data is collected on Pb-free electronics mitigation efforts, the documented results will need to be compiled, analyzed and added as part of a continually updated Pb-free electronics research and development program.

### **Develop a communication package to brief the customers.**

Through the efforts of the B2PCOE, the PERM, and other consortium, a concerted, organized communications plan is needed to train providers and vendors about the best Pb-free manufacturing practices, and offer a briefing on the specifics of the technological roadmap.

### **Use the Lead Free Electronics Manhattan Project model for other industry-pervasive issues.**

The model for conducting the Lead Free Electronics Manhattan Project has proven to be a successful method for integrating a diverse body of subject matter experts and creating an environment of synthesized information exchange and capture. It is recommended that this process be identified as a best practice and applied to other pervasive issues.

“There are risks and costs to a program of action.

But they are far less than the long-range risks and costs  
of comfortable inaction.”

*—John F. Kennedy (1917-1963)*





# Appendix A

## CHAPTER 2 SUPPLEMENTAL INFORMATION

The PERM Consortium framework includes a Research Coordination Task Team chartered to define, develop, and maintain an overall systematic, coordinated plan to provide the necessary research and development to address all the critical needs of the aerospace and defense community regarding the global transition to lead-free electronics. Comprised of volunteer members from government, industry and academia, the Research Coordination Task Team has no current budget or funding capabilities, and is only able to coordinate known and recommended R&D activities, and endeavor to minimize overlap and duplication of efforts across the participating organizations. As portrayed in Figure A.2.1 the Research Coordination Task Team will include the Lead Free Electronics Manhattan Project as one of the R&D activities that it coordinates with, in addition to other government, industry and academic Pb-free electronics R&D projects that are either underway or being planned.

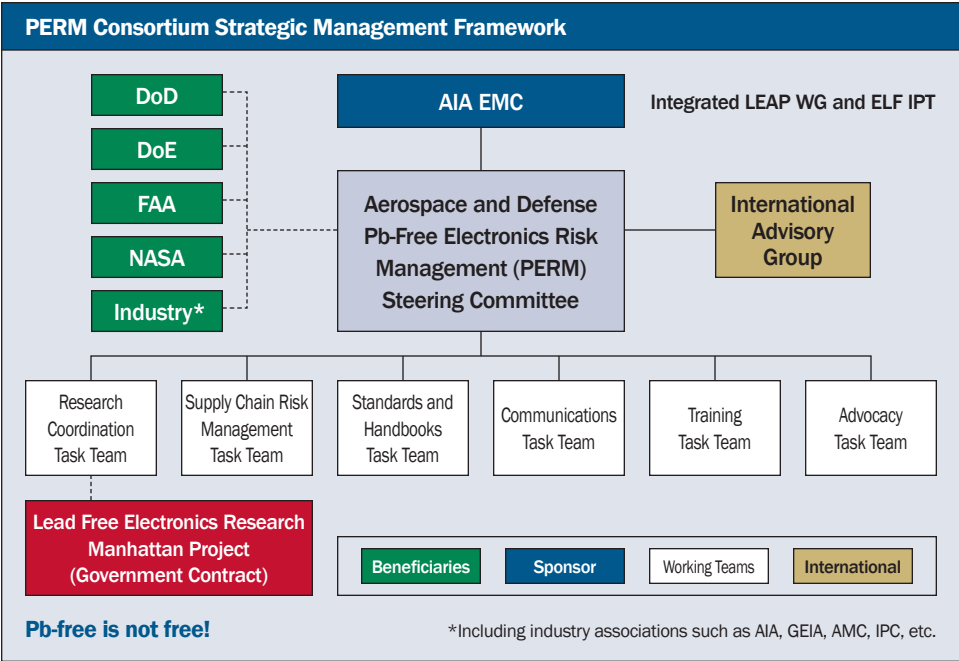


Figure A.21 PERM Consortium Strategic Framework. The Pb-free Electronics Risk Management (PERM) Consortium is comprised of government, industry and academia representatives focused on mitigating Pb-free electronics risks.



## CHAPTER 4 SUPPLEMENTAL INFORMATION

Package Thickness	Volume mm <sup>3</sup> < 350	Volume mm <sup>3</sup> ≤ 350
< 2.5 mm	240 +0/-5 °C	225 +0/-5 °C
≥ 2.5 mm	225 +0/-5 °C	225 +0/-5 °C

Table A.4.1 SnPb Eutectic Process – Package Peak Reflow Temperatures

Package Thickness	Volume mm <sup>3</sup> < 350	Volume mm <sup>3</sup> 350-2000	Volume mm <sup>3</sup> > 2000
< 1.6 mm	260 +0 °C*	260 +0 °C*	260 +0 °C*
1.6 mm - 2.5 mm	260 +0 °C*	250 +0 °C*	245 +0 °C*
≥ 2.5 mm	250 +0 °C*	245 +0 °C*	245 +0 °C*

\*Tolerance: The device manufacturer/supplier **shall** assure process compatibility up to and including the stated classification temperature (this means peak reflow temperature +0 °C. For example, 260 °C+0 °C) at the rated MSL level.

Table A.4.2 Pb-Free Process – Package Classification Reflow Temperatures

**Note 1:** The profiling tolerance is +0 °C, -X °C (based on machine variation capability) whatever is required to control the profile process but at no time will it exceed -5 °C. The producer assures process compatibility at the peak reflow profile temperatures defined in Table A.4.2.

**Note 2:** Package volume excludes external terminals (balls, bumps, lands, leads) and/or nonintegral heat sinks.

**Note 3:** The maximum component temperature reached during reflow depends on package thickness and volume. The use of convection reflow processes reduces the thermal gradients between packages. However, thermal gradients due to differences in thermal mass of SMD packages may still exist.

**Note 4:** Components intended for use in a “lead-free” assembly process **shall** be evaluated using the “lead-free” classification temperatures and profiles defined in Tables A.4.1 and A.4.2 whether or not lead-free.

CHAPTER 6 SUPPLEMENTAL INFORMATION

Table A.6.1 Specification and Standard Table

Baseline Practice	Test and Applicable Standard	Is the Current Test Equipment Adequate for Pb-Free?	Are the Current Test Parameters Adequate for Pb-Free?	Comments
Solderability (Dip and Look, Wave Solder)	IPC J-STD-003B "Solderability for Printed Boards," March 2007	Yes	Yes	Specifies using SAC305 solder and paste. "Other lead-free solder alloys upon agreement between user and vendor."
Electromigration Testing	IPC-TM-650, Method 2.6.14.1F, "Electrochemical Migration Resistance Test," September 2000	Yes	Yes	This test method provides a means to assess the propensity for surface electrochemical migration. This test method can be used to assess soldering materials and/or processes.
PCB Tin Whiskers	No Industry Standard Test Method Exists	No	No	PC-4554 states "...the test method will be used with the understanding that the responsibility to verify the impact of potential whisker growth on a module's long term reliability is the end users. See Appendix 6 for JEDEC/IPC PCB paragraphs."
Surface Finish Verification (XRF)	MIL-STD-1580 (Draft), "Detailed Requirements for Prohibited Materials Analysis and Incoming Inspection of External Package Plating Materials Using X-Ray Fluorescence Spectroscopy or Scanning Electron Microscopy with Energy Dispersive Spectroscopy"	Yes (Draft)	Yes (Draft)	Specification is a draft.

Baseline Practice	Test and Applicable Standard	Is the Current Test Equipment Adequate for Pb-Free?	Are the Current Test Parameters Adequate for Pb-Free?	Comments
PCB Delamination Test	IPC-TM-650, Method 2.4.24.1, "Time to Delamination," December 1994	Yes	With Modifications	"This method describes the method for determining the time to delamination of laminates and PCBs through the use of a thermomechanical analyzer (TMA)."
	IPC-TM-650, Method 2.4.13.1, "Thermal Stress of Laminates," December 1994	Yes	With Modifications	"This test method is designed to determine the thermal integrity of unclad or metallic clad laminates using short-term solder exposure."
	IPC-TM-650, Method 2.4.23, "Soldering Resistance of Laminate Materials," March 1979	Yes	With Modifications	Specifies SnPb in test. "This test method is used to determine the resistance of laminate materials (both unclad and etched surfaces) to the thermal abuse of a solder dip."
PCB Conductive Anodic Filament (CAF)	IPC-TM-650, Method 2.6.25, "Conductive Anodic Filament Resistance Test:X-Y Axis," November 2003	Yes	With Modifications	Does not discuss exposure to thermal environments before test.
PCB Interconnect Stress Testing (IST)	PC-TM-650, Method 2.6.26, "DC Current Induced Thermal Cycling Test," November 1999	Yes	Yes	Currently used for Pb-free per specifications in IPC 6012 for bare PCBs.
Cu Dissolution Test	No Industry Standard Test Method Exists	No	No	Industry practice exists.

## Appendix A

Baseline Practice	Test and Applicable Standard	Is the Current Test Equipment Adequate for Pb-Free?	Are the Current Test Parameters Adequate for Pb-Free?	Comments
PCB Copper Test, Electrodeposited Copper	IPC-2.4.18.1, "Tensile Strength and Elongation, In-House Plating," May 2004	Yes	Yes	To determine the tensile strength in MPa (psi) and the elongation, in percentage, of electrodeposited copper plating at ambient temperatures by mechanical force testing.
PCB Copper Test, Copper Foil	IPC-2.4.18, "Tensile Strength and Elongation, Copper Foil," August 1980	Yes	Yes	To determine the tensile strength in MPa (psi) and the elongation, in percentage, of copper foil at ambient and elevated temperatures by mechanical force testing.
Surface Finish Verification (XRF)	MIL-STD-1580 (Draft), "Detailed Requirements for Prohibited Materials Analysis and Incoming Inspection of External Package Plating Materials Using X-Ray Fluorescence Spectroscopy or Scanning Electron Microscopy with Energy Dispersive Spectroscopy"	Yes (Draft)	Yes (Draft)	Specification is a draft.
Component Solderability	IPC/EAC J-STD-002C, "Solderability Tests for Component Leads, Terminations, Lugs, Terminals and Wires," November 2008	Yes	Yes	This standard prescribes test methods, defect definitions, acceptance criteria, and illustrations for assessing the solderability of electronic component leads, terminations, solid wires, stranded wires, lugs, and tabs. This standard also includes a test method for the Resistance to Dissolution/Dewetting of Metallization. This standard is intended for use by both vendor and user.

Baseline Practice	Test and Applicable Standard	Is the Current Test Equipment Adequate for Pb-Free?	Are the Current Test Parameters Adequate for Pb-Free?	Comments
Component Tin Whisker Assessment	JESD22-A121A, "Test Method for Measuring Whisker Growth on Tin and Tin Alloy Surface Finishes," July 2008	No	No	This test method may not be sufficient for applications with special requirements, e.g., military or aerospace.
	JESD-201, "Environmental Acceptance Requirements for Tin Whisker Susceptibility of Tin and Tin Alloy Surface Finishes," September 2008	No	No	This test method may not be sufficient for applications with special requirements, e.g., military or aerospace. The uncertainty of the Sn whisker growth incubation period (hours to years) confounds qualification tests for surface finishes on printed circuit boards, components and circuit card assemblies.
Paste Solderability Testing	IPC-TM-650, Method 2.4.46 Rev.A, "Spread Test, Liquid, Paste or Solid Flux, or Flux Extracted from Solder Paste, Cored Wires or Performs," June 2004	Yes	With Modifications	Specifies using Sn60 solder.
	IPC-TM-650, Method 2.4.45, "Solder Paste – Wetting Test," January 1995	Yes	With Modifications	Does not mention solder type.
Surface Insulation Resistance (SIR)	IPC-TM-650, Method 2.6.3.3 Rev. B, "Surface Insulation Resistance, Fluxes," June 2004	Yes	Yes	
Tin Pest	No Industry Standard Test Method Exists	No	No	Current industry practice is an isothermal hold at -40°C until tin pest is observed.

Appendix A

Baseline Practice	Test and Applicable Standard	Is the Current Test Equipment Adequate for Pb-Free?	Are the Current Test Parameters Adequate for Pb-Free?	Comments
Solder Joint Tin Whisker Assessment	No Industry Standard Test Method Exists	No	No	SAC solder joints have been observed to grow whiskers. The addition of trace elements (Ce, etc.) to SAC may promote whisker growth.
Stabilization and Other Annealing Treatments	IPC-9701A, "Performance Test Methods and Qualification Requirements for Surface Mount Solder Attachments," February 2006	Yes	With Modifications	Establish stabilization treatments based upon microstructure kinetics, for each alloy. Isothermal annealing treatments may also be required to simulate follow-on manufacturing and test conditions as well as harsh service environments.
Time Independent Monotonic (Stress Strain) Mechanical Properties	ASTM E8/E8M - 08 Standard Test Methods for Tension Testing of Metallic Materials	Yes	With Modifications	In the case of testing solder alloys, the standard test specimen geometries do not address microstructure size scale effects. It is recommended that alternative, smaller sample geometries be considered.
	ASTM E21 - 05 Standard Test Methods for Elevated Temperature Tension Tests of Metallic Materials	Yes	With Modifications	In the case of testing solder alloys, the standard test specimen geometries do not address microstructure size scale effects. It is recommended that alternative, smaller sample geometries be considered.

Baseline Practice	Test and Applicable Standard	Is the Current Test Equipment Adequate for Pb-Free?	Are the Current Test Parameters Adequate for Pb-Free?	Comments
	ASTM E209 - 00 (2005) Standard Practice for Compression Tests of Metallic Materials at Elevated Temperatures with Conventional or Rapid Heating Rates and Strain Rates	Yes	With Modifications	In the case of testing solder alloys, the standard test specimen geometries do not address microstructure size scale effects. It is recommended that alternative, smaller sample geometries be considered.
	ASTM E111 - 04 Standard Test Method for Young's Modulus, Tangent Modulus, and Chord Modulus	Yes	With Modifications	In the case of testing solder alloys, the standard test specimen geometries do not address microstructure size scale effects. It is recommended that alternative, smaller sample geometries be considered.
	ASTM E143 - 02 (2008) Standard Test Method for Shear Modulus at Room Temperature	Yes	With Modifications	In the case of testing solder alloys, the standard test specimen geometries do not address microstructure size scale effects. It is recommended that alternative, smaller sample geometries be considered.
	ASTM E1876 - 07 Standard Test Method for Dynamic Young's Modulus, Shear Modulus, and Poisson's Ratio by Impulse Excitation of Vibration	Yes	With Modifications	In the case of testing solder alloys, the standard test specimen geometries do not address microstructure size scale effects. It is recommended that alternative, smaller sample geometries be considered.

Appendix A

Baseline Practice	Test and Applicable Standard	Is the Current Test Equipment Adequate for Pb-Free?	Are the Current Test Parameters Adequate for Pb-Free?	Comments
	ASTM C1273 - 05 Standard Test Method for Tensile Strength of Monolithic Advanced Ceramics at Ambient Temperatures	Yes	Yes	
	ASTM C1366 - 04 Standard Test Method for Tensile Strength of Monolithic Advanced Ceramics at Elevated Temperatures	Yes	Yes	
	ASTM D638 - 08 Standard Test Method for Tensile Properties of Plastics	Yes	Yes	
	ASTM E345 - 93 (2008) Standard Test Methods of Tension Testing of Metallic Foil	Yes	Yes	
Time Dependent Monotonic (Creep) Mechanical Properties	ASTM E139 - 06 Standard Test Methods for Conducting Creep, Creep-Rupture, and Stress-Rupture Tests of Metallic Materials	Yes	With Modifications	In the case of testing solder alloys, the standard test specimen geometries do not address microstructure size scale effects. It is recommended that alternative, smaller sample geometries be considered.
	ASTM E328 - 02 (2008) Standard Test Methods for Stress Relaxation Tests for Materials and Structures	Yes	With Modifications	In the case of testing solder alloys, the standard test specimen geometries do not address microstructure size scale effects. It is recommended that alternative, smaller sample geometries be considered.



Baseline Practice	Test and Applicable Standard	Is the Current Test Equipment Adequate for Pb-Free?	Are the Current Test Parameters Adequate for Pb-Free?	Comments
	ASTM E1457 - 07e1 Standard Test Method for Measurement of Creep Crack Growth Times in Metals	Yes	With Modifications	In the case of testing solder alloys, the standard test specimen geometries do not address microstructure size scale effects. It is recommended that alternative, smaller sample geometries be considered.
Cyclic Mechanical Properties (Isothermal)	ASTM E606 - 04e1 Standard Practice for Strain-Controlled Fatigue Testing	Yes	With Modifications	In the case of testing solder alloys, the standard test specimen geometries do not address microstructure size scale effects. It is recommended that alternative, smaller sample geometries be considered.
	ASTM E468 - 90 (2004) e1 Standard Practice for Presentation of Constant Amplitude Fatigue Test Results for Metallic Materials	Yes	With Modifications	In the case of testing solder alloys, the standard test specimen geometries do not address microstructure size scale effects. It is recommended that alternative, smaller sample geometries be considered.
Material Physical Properties	ASTM E831 - 06 Standard Test Method for Linear Thermal Expansion of Solid Materials by Thermomechanical Analysis	Yes	With Modifications	Specimen geometry/ microstructure size scale effects may need to be considered with respect to sample size versus polycrystalline versus polycrystalline grain size.

Appendix A

Baseline Practice	Test and Applicable Standard	Is the Current Test Equipment Adequate for Pb-Free?	Are the Current Test Parameters Adequate for Pb-Free?	Comments
	ASTM E289 - 04 Standard Test Method for Linear Thermal Expansion of Rigid Solids with Interferometry	Yes	With Modifications	Specimen geometry/ microstructure size scale effects may need to be considered with respect to sample size versus polycrystalline versus polycrystalline grain size.
	ASTM E228 - 06 Standard Test Method for Linear Thermal Expansion of Solid Materials with a Push-Rod Dilatometer	Yes	With Modifications	Specimen geometry/ microstructure size scale effects may need to be considered with respect to sample size versus polycrystalline versus polycrystalline grain size.
	ASTM E1545 - 05 Standard Test Method for Assignment of the Glass Transition Temperature by Thermomechanical Analysis	Yes	With Modifications	Specimen geometry/ microstructure size scale effects may need to be considered with respect to sample size versus polycrystalline versus polycrystalline grain size.
Failure Mode Analysis of Materials Test Specimens	IPC-TM-650, Method 2.1.1 Rev. E, "Micro-sectioning, Manual Method," May 2004	Yes	Yes	No change in current micro-sectioning techniques required. Focused ion beam (FIB) techniques may be required to see some features.

Baseline Practice	Test and Applicable Standard	Is the Current Test Equipment Adequate for Pb-Free?	Are the Current Test Parameters Adequate for Pb-Free?	Comments
Time Independent Monotonic (Stress Strain) Mechanical Properties	ASTM D3165 - 07 Standard Test Method for Strength Properties of Adhesives in Shear by Tension Loading of Single-Lap-Joint Laminated Assemblies	Yes	No	The solder joint geometry (footprint and gap thickness) must be clearly defined and should consider the microstructure size scale effects. It is critical that the compliance of the load train be fully taken into account in order to correctly analyze and interpret the data.
	ASTM D3528 - 96 (2008) Standard Test Method for Strength Properties of Double Lap Shear Adhesive Joints by Tension Loading	Yes	No	The solder joint geometry (footprint and gap thickness) must be clearly defined and should consider the microstructure size scale effects. It is critical that the compliance of the load train be fully taken into account in order to correctly analyze and interpret the data.
Time Dependent Monotonic (Creep) Mechanical Properties	ASTM D2294 - 96 (2008) Standard Test Method for Creep Properties of Adhesives in Shear by Tension Loading (Metal-to-Metal)	Yes	No	The solder joint geometry (footprint and gap thickness) must be clearly defined and should consider the microstructure size scale effects. It is critical that the compliance of the load train be fully taken into account in order to correctly analyze and interpret the data.

## Appendix A

Baseline Practice	Test and Applicable Standard	Is the Current Test Equipment Adequate for Pb-Free?	Are the Current Test Parameters Adequate for Pb-Free?	Comments
	ASTM D2293 - 96 (2008) Standard Test Method for Creep Properties of Adhesives in Shear by Compression Loading (Metal-to-Metal)	Yes	No	The solder joint geometry (footprint and gap thickness) must be clearly defined and should consider the microstructure size scale effects. It is critical that the compliance of the load train be fully taken into account in order to correctly analyze and interpret the data.
Cyclic Mechanical Properties (Isothermal)	No Industry Standard Test Method Exists	Yes	No	The solder joint geometry (footprint and gap thickness) must be clearly defined and should consider the microstructure size scale effects. It is critical that the compliance of the load train be fully taken into account in order to correctly analyze and interpret the data.
Failure Mode Analysis of Simulated Solder Joints	IPC-TM-650, Method 2.1.1 Rev. E, "Microsectioning, Manual Method," May 2004	Yes	Yes	No change in current micro-sectioning techniques required. Focused ion beam (FIB) techniques may be required to see some features.
Humidity Testing	MIL-STD-810G, Method 507.5, "Environmental Engineering Considerations and Laboratory Tests," October 31, 2008	Yes	Yes	

Baseline Practice	Test and Applicable Standard	Is the Current Test Equipment Adequate for Pb-Free?	Are the Current Test Parameters Adequate for Pb-Free?	Comments
Thermal Shock	MIL-STD-810G, Method 503.5, "Environmental Engineering Considerations and Laboratory Tests," October 31, 2008	Yes	No	IPC-SM-785 cautions that thermal shock cycling can induce failure mechanisms not seen in thermal cycling due to warping of the test vehicle. IPC-SM-785 recommends that thermal shock cycling not be used for testing unless the intent is to simulate a thermal shock environment.
Thermal Cycling (For ESS, Verification, Validation, and Qualification Testing)	IPC-SM-785, "Guidelines for Accelerated Reliability Testing of Surface Mount Solder Attachments," November 1992	Yes	No	For production hardware, the choice of thermal cycle test parameters (temperature deltas, ramp rates, and dwell times) should be chosen so that the test is equivalent to a specific time in the field. This will require mathematical models that can convert the expected field conditions into accelerated test conditions.
	IPC-9701A, "Performance Test Methods and Qualification Requirements for Surface Mount Solder Attachments," February 2006	Yes	No	
	GEIA-STD-0005-3, Performance Testing for Aerospace and High Performance Electronic Interconnects Containing Pb-free Solder and Finishes, June 2008	Yes	No	

Appendix A

Baseline Practice	Test and Applicable Standard	Is the Current Test Equipment Adequate for Pb-Free?	Are the Current Test Parameters Adequate for Pb-Free?	Comments
Vibration Testing (For ESS, Verification, Validation, and Qualification Testing)	MIL-STD-810G, Method 514.6, "Environmental Engineering Considerations and Laboratory Tests," October 31, 2008	Yes	No	For production hardware, the choice of vibration test parameters (PSD levels and test durations) should be chosen so that the test is equivalent to a specific time in the field. This will require mathematical models that can convert the expected field conditions into accelerated test conditions.
Mechanical Shock Testing (For Verification, Validation, and Qualification Testing)	MIL-STD-810G, Method 516.6, "Environmental Engineering Considerations and Laboratory Tests," October 31, 2008	Yes	No	For production hardware, the shock pulse or SRS (Shock Response Spectrum) input parameters will be defined by the individual program.
	IPC/JEDEC-9703, "Mechanical Shock Test Guidelines for Solder Joint Reliability," March 2009	Yes	No	
Isothermal Aging	No Industry Standard Test Method Exists	No	No	

Baseline Practice	Test and Applicable Standard	Is the Current Test Equipment Adequate for Pb-Free?	Are the Current Test Parameters Adequate for Pb-Free?	Comments
Combined Environments (HALT, HAST)	GMW8287, "Highly Accelerated Life Testing," February 1, 2002	Yes	No	Validated mathematical models for converting combined environment test results into field lifetimes probably do not exist. Therefore, HALT is best used as a screening test for uncovering defects and weak spots in a design and not as a tool for determining reliability. HALT PSD inputs are often not well characterized, which means that the resonance frequencies of the test article can be excited more (or less) than anticipated resulting in over-testing or under-testing of the test article.
	JESD-22-A110C, "Highly Accelerated Temperature and Humidity Stress Test (HAST)," January 2009	Yes	No	

Appendix A

Baseline Practice	Test and Applicable Standard	Is the Current Test Equipment Adequate for Pb-Free?	Are the Current Test Parameters Adequate for Pb-Free?	Comments
Electromigration Testing (Small Solder Balls)	No Industry Standard Test Method Exists	No	No	As the size of solder joints decrease (e.g., the diameter of solder balls is approaching 50 microns), electromigration may become a reliability issue due to void formation. No standardized test method exists for conducting this testing.
Failure Mode Analysis of Test Vehicles	IPC-TM-650, Method 2.1.1 Rev. E, "Microsectioning, Manual Method," May 2004	Yes	Yes	No change in current micro-sectioning techniques required. Focused ion beam (FIB) techniques may be required to see some features.
Black Pad, Kirkendall Voids, Pad Cratering, Pad Lifting, Trace Cracking	No Industry Standard Test Method Exists	No	No	Intel is developing a pad cratering test.

Table A.6.1 Specification and Standard Table

A.6.3 Material Testing for Computational Modeling

Computational modeling provides the means to predict the long-term fatigue performance of Pb-free solder interconnections in place of extensive laboratory test programs. Modeling is advantageous to both the design and reliability engineer because of the growing range of materials sets, solder joint geometries, and test. Likewise, service environments of today's high-reliability electronics have caused large-scale, CCA experimental programs to be cost ineffective and schedule prohibitive. Modeling approaches predict Pb-free interconnection reliability through deterministic calculations of cycles-to-failure as well as quantify uncertainty by determining the effects of solder joint geometry variations and materials properties ranges.



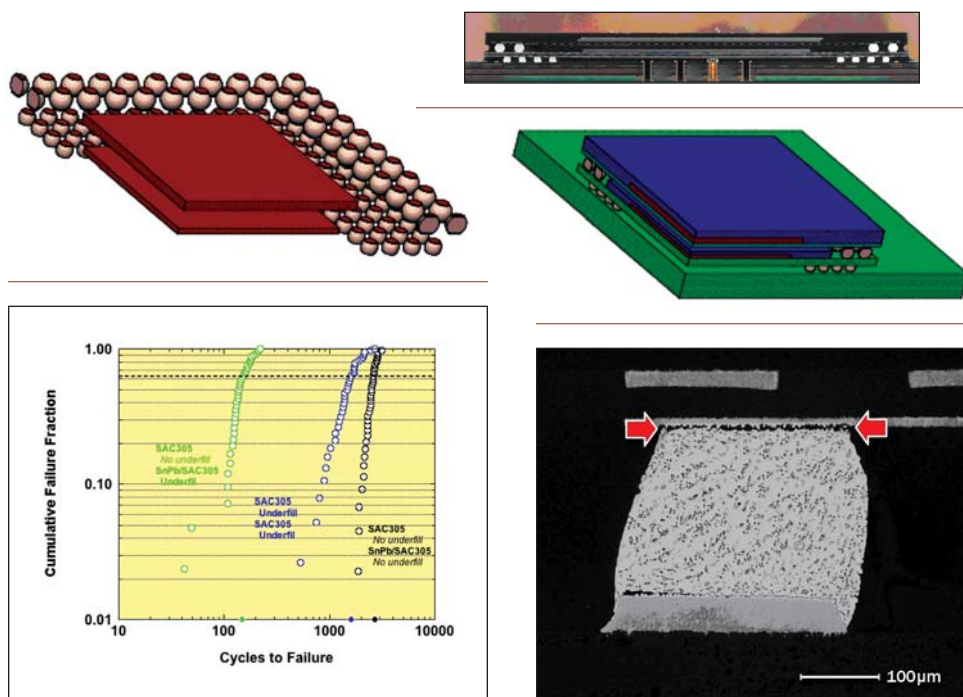


Figure A.6.1 Computational model of package-on-package Pb-free solder joint fatigue.

Computational models readily determine hardware test parameters for (a) verification, (b) validation, (c) qualification, or (d) acceptance of Pb-free solder interconnections that, more importantly, can now be based upon actual service lifetimes rather than only “lower bounds” benchmarks as provided by current specifications. This approach avoids the pitfalls of either under-testing the interconnections, resulting in a reliability shortfall, or over-testing the interconnections, which results in early failures that lead to hardware over-design and excessive product scrap. The modeling approach provides the basis to make “accept/reject” decisions in a cost-effective, time-efficient manner for Pb-free interconnections.

The fidelity of computational modeling predictions is dependent upon the accuracy of the mechanical and physical properties of the materials used to construct the interconnection – solder as well as substrate laminate and component package materials (e.g., ceramic, plastic, etc.). In particular, it is becoming necessary to determine the effects of substrate and surface finish dissolution on the mechanical and physical properties of the solder, given the trend towards increasingly smaller interconnection sizes. Standardized materials testing programs are required in order to provide accurate mechanical and physical materials properties as input data for the computational models.

In addition, materials testing methods can provide the first steps towards validation of the computational model predictions. The materials test data – stress-strain curves, strain-time curves (creep), and hysteresis loops (isothermal fatigue) – provide a first-level validation of the constitutive equation by comparing calculated test curves against the respective empirical curves as a function of temperature, strain rate, etc. Secondly, the data obtained from the testing of simulated solder joints provides validation of the combined constitutive equation and finite element functions within the model. The relatively simple, easy-to-make test specimens allow for evaluating a wide range of test parameters against which to exercise the computational model.

### A.6.3.1 Stabilization and Other Annealing Treatments

Mechanical and physical properties of metal alloys are sensitive to the as-solidified microstructure (grain size, dislocation density, etc.). Stabilizing the material microstructure prior to testing can reduce the variability of those measured properties.

In many circumstances, solder joints are exposed to additional elevated temperature environments prior to, as well as during, service lifetimes. Isothermal annealing treatments can be used to simulate such exposures so that the measured material mechanical and physical properties reflect the altered microstructure.

The recommended stabilization conditions (air) for several solders are listed below:

- 100 °C, 24 hours for 63Sn37Pb ( $T_{eut} = 183\text{ °C}$ ) or 60Sn40Pb alloys
- 125 °C, 24 hours for SnAgCu ( $T_{eut} = 217\text{ °C}$ ) and SnCuX alloys
- 75 °C, 24 hours for 97In3Ag ( $T_{eut} = 149\text{ °C}$ ) alloy
- 50 °C, 24 hours for 52In48Sn ( $T_{eut} = 118\text{ °C}$ ) alloy

These parameters are currently based upon a homologous temperature of 0.8 as defined for SnPb eutectic solder by AT&T (100 °C, 24 hours), not the stabilization process rate kinetics of each solder, which is the preferred approach. *Following the stabilization or other annealing treatment, metallographic cross section techniques should be used to document the resulting microstructure that serves as the “initial condition” of the following test regiments. The as-cast microstructure should be similarly documented prior to any of the following tests.*

### A.6.3.2 Time Independent Monotonic (Stress-Strain) Mechanical Properties

Accurate time independent, monotonic (stress-strain) mechanical properties are required of the Pb-free solder, the substrate, and the component construction materials in order to maximize the fidelity of the computational model predictions. Test temperatures and strain-rates must bound those anticipated for the interconnections when exposed to service and all test conditions. The starting microstructure should be documented by metallographic cross section techniques.

The determined properties of yield strength, ultimate strength, Poisson's ratio, work hardening or work softening parameters, and static modulus properties provide input parameters for the constitutive model. The stress-strain curves can be used to validate the constitutive equation of the model. The relevant ASTM test methods are listed in Table A.6.1. *An alternative technique to obtain the elastic and shear moduli as well as Poisson's ratio, is by means of pulsed vibration. These parameters are then referred to as dynamic properties (rather than static properties).* All solder compositions can be evaluated by these methods because the test procedures are considered universal for metallic materials.

#### A.6.3.3 Time Dependent Monotonic (Creep) Mechanical Properties

High fidelity computational model predictions require an accurate knowledge of the time-dependent (creep) deformation properties of the solder as well as similar deformation within the substrate and component construction materials. Test temperatures and applied loads or stresses must bound those anticipated for the interconnections under service and all test conditions. The starting microstructure should be documented by metallographic cross section techniques

The rate kinetics is determined from the secondary or steady-state portion of the creep tests. The important kinetics parameters are the power law stress exponent (or sinh term exponent) and the apparent activation energy. The strain-time curves are compared to the computational model prediction as a means to validate the constitutive equation. The relevant ASTM test methods are listed in Table A.6.1. All solder compositions can be evaluated by these methods as the latter are considered universal for metallic materials.

#### A.6.3.4 Cyclic Mechanical Properties (Isothermal)

Cyclic (isothermal) test data are used to validate the constitutive equation's response to fatigue deformation of the solder or other material. It is important that test temperatures, strain rates, as well as the strain limits (strain controlled) bound those expected of the interconnections under service and all test conditions. The starting microstructure should be documented by metallographic cross section techniques.

The parameters obtained from such tests are the hysteresis loop strain energy as well as the percent load-change (drop or rise) as a function of cycle. In particular, the latter data are needed at 25%, 50%, 75%, and 100% load change. The relevant ASTM test methods are listed in Table A.6.1. All solder compositions can be evaluated by these standard methods as they are considered universal for metallic materials.

#### A.6.3.5 Material Physical Properties

Accurate physical properties data are required to maximize the fidelity of the computational model predictions. The critical physical property required by the computational models is the coefficient of thermal expansion. It is necessary that the CTE be measured over the temperature range

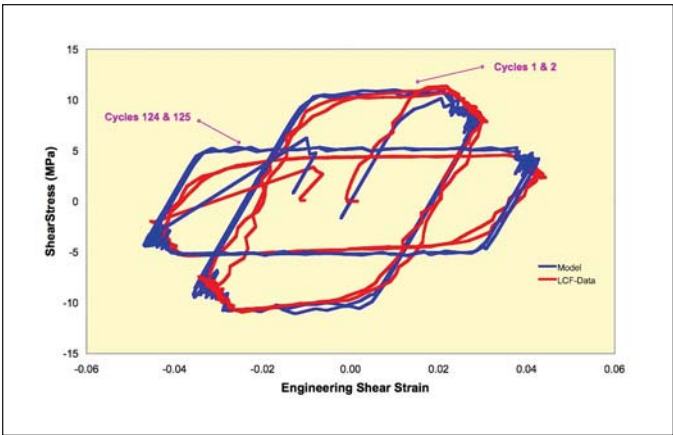
expected of both test and service lifetime environments in order to capture any abrupt or, otherwise unexpected changes caused by microstructure changes (e.g., phase changes). The starting microstructure should be documented by metallographic cross section techniques. The relevant ASTM test methods are listed in Table A.6.1. All solder compositions can be evaluated by these methods.

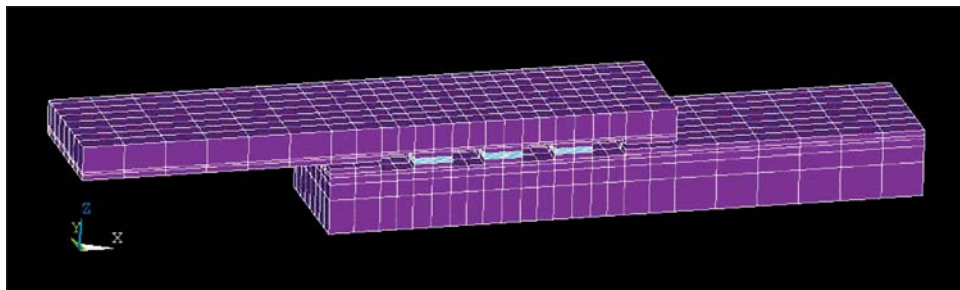
A.6.3.6 Failure Mode Analysis of Materials Test Specimens

It is critical that the materials testing processes be followed by a thorough failure mode analyses. Metallographic cross sections are critical towards revealing the post-test microstructure. Scanning electron microscopy is used to assess fracture surfaces. Those analyses provide a map of failure mode versus stress, strain, strain rate, and temperature against which to compare alloy deformation and damage in the joint configuration when subjected to more complex loading conditions, including test and product vehicle interconnections. Traditional metallographic cross sectioning, grinding, and polishing techniques provide the basis from which to perform Pb-free solder sample preparation steps.

A.6.3.7 Simulated Solder Joint Testing

The testing of simulated Pb-free solder joints provides an avenue of intermediate complexity with which to validate both the constitutive equation and finite element functions of the computational model. The relatively simple specimen geometries allow for the fabrication and testing of many samples in order to provide a range of starting microstructures and test conditions against which to compare the output of the exercised model at minimal cost.





*Figure A.6.2 Double lap shear simulated solder joint.*

The numerous requirements that were described previously for the materials testing are equally applicable here for simulated solder joint testing, include the use of test temperatures that bound both test and service conditions, strains ranges, strain rates, and applied stresses. It is necessary to perform metallographic cross sections of the samples prior to testing to document that initial microstructure.

The most relevant ASTM test methods are listed in Table A.6.1. There are no standardized tests for solder joints. These aforementioned tests were developed for measuring the properties of adhesive joints. The specimens and procedures provide a starting-point for such test regiments because solder joints are similar to adhesive joints since the filler material (solder versus adhesive) is considerably weaker than the base material. Nevertheless, the lack of standards controls for simulated solder joint testing necessitates an increased rigor towards reporting specimen geometries, starting microstructures, and test parameters.

The tests can be performed so as to subject the Pb-free solder joint to shear or tension/compression loads.

The testing of simulated solder joints must consider machine and specimen base material compliance as they can potentially impact the test conditions at the actual solder joint(s) and the resulting stress and strain data that is measured from such tests. This point is particularly true of the stronger Pb-free solders vis-à-vis SnPb alloys.

All solder compositions can be evaluated by these methods. However, additional precautions are required with respect to achieving minimal void formation in the solder joints. This is a particular concern with Pb-free solders, which have a more limited solderability than the SnPb solders. X-ray and scanning acoustic microscopy techniques should be used to document void formation prior to performing the test.

The particular test regiments are listed below with the section number that is relevant to Table A.6.1.

- Time Independent Monotonic (Stress-Strain) Mechanical Properties – A.6.3.2 (also 6.3.2)
- Time Dependent Monotonic (Creep) Mechanical Properties – A.6.3.3 (also 6.3.3)
- Cyclic Mechanical Properties (Isothermal) – A.6.3.4 (also 6.3.4)
- Failure Mode Analysis of Simulated Solder Joints – A.6.3.6 (also 6.3.8)

It is critical that the materials testing processes be followed up by thorough failure mode analyses of the Pb-free solder joints. Those analyses provide a materials performance database with which to compare deformation and damage of the Pb-free alloy in the joint configuration under complex loading conditions as determined by the test conditions. Prior to metallographic cross sections, consideration should be given to using scanning electron microscopy to document the fracture surfaces, which are not well characterized for Pb-free solders. Traditional metallographic cross sectioning, grinding, and polishing techniques provide the basis for sample preparation procedures.

CHAPTER 7 SUPPLEMENTAL INFORMATION

The following has been culled from publications under preparation by Unovis Solutions and Binghamton University (BU) and reflects only the view of those authors [52, 53]. As outlined here, they suggest that, depending on the product and service conditions of concern, current best assessments of the life in service may be in error by up to ten times or more. In fact, even relative comparisons of alternatives done for the purpose of design, materials, or process optimization may easily become misleading. Figure A.7.1 shows an example where the ranking of SAC alloys depends on the choice of (both relatively short) dwell times in cycling.

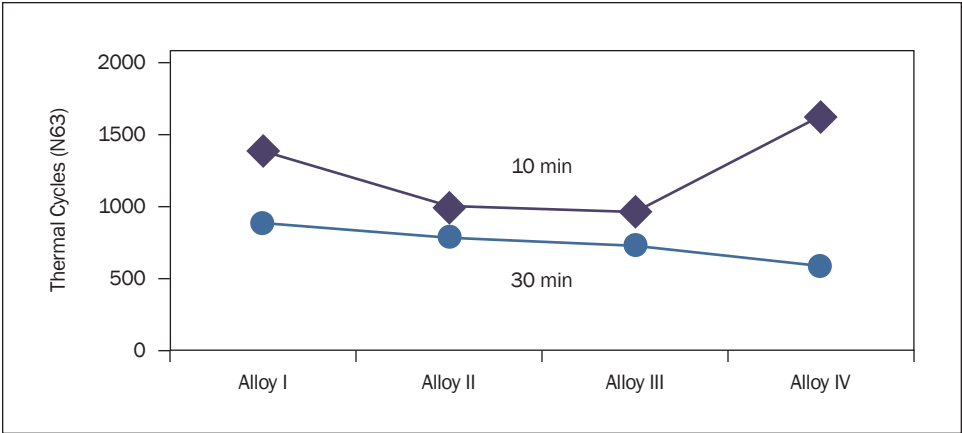


Figure A.7.1 Effect of dwell time in thermal cycling. Number of cycles to failure for four different SAC alloys in 0/100 °C cycling of BGAs with 10 minute and 30 minute dwells, respectively. Courtesy of Unovis.

None of the currently available models account for effects of solder joint volume, pad finishes, aging effects, reflow process details and other thermal history on solder joint microstructure and properties. These factors have all been shown to affect the solder microstructure, and thus the properties, significantly. In addition, neither the leadless Engelmaier model nor any of the Norris Landzberg variants account for the effect of pad size or joint diameter, and thus for how long a crack has to become to be fatal. The only credible approach to the assessment of life in service of a particular CCA is therefore an extrapolation of one or more accelerated test results for the assembly, process, reworks, etc, in question.

This means that we are concerned with the level of confidence we may have in the acceleration factors from test to service conditions. A thermal cycling test is characterized by heating and cooling rates, maximum and minimum temperatures, and the durations of the dwell or “soak” at either temperature. Prediction of life in service requires the extrapolation of test results along dependencies on each of these.

It is not surprising that current models tend to reproduce common accelerated test results and acceleration factors from one test to another quite well. However, systematic effects are being ignored. Unovis/BU do, for example, report systematic effects of solder joint dimensions. In one experiment, the acceleration from 0/100°C to -40/125°C cycling increased systematically from two to five times when the solder ball diameter was reduced from 30mil to 10mil.

In the following, the original Norris Landzberg model was evaluated using parameters proposed by [17] Vasudevan and Fan (NL-0), while the modified Norris Landzberg model was evaluated using parameters proposed by [18] Pan et al. (NL-1) and by [20] Dauksher (NL-2). Predictions by the Engelmaier model were calculated based on parameters proposed by CALCE [14].

We are aware of two examples of experiments leading to acceleration factors from 0/100°C cycling to 25/75°C cycling without change of ramp rates or dwell times. CALCE [53] found a factor of ten times with a 15 minute dwell while Unovis/BU reports six times for very high strains and a five minute dwell. With one exception (NL-1), the above models predicted acceleration factors of 4.6-5.7 times.

However, Unovis/BU also reported examples of dwell time dependencies that were much stronger than predicted by any of the models. Thus, one case life was reduced by three times when the dwell time was extended from 10 minutes to two hours. Engelmaier and NL-1 predicted 1.4 times, NL-2 and NL-0 a factor of 1.9 times. The Engelmaier model will thus underestimate the acceleration factors for some applications by at least two times, but the projected difference is worse.

Dauksher (NL-2) and the Finite Element Modeling of Dasgupta [10,57] demonstrate that current creep constitutive models predict creep saturation after approximately 20 minutes at 125 °C in Sn37Pb BGA solder joints but do not predict a similar saturation in SAC305 BGA joints for up to three hours of hot dwell at 125 °C. The other Norris Landzberg models and Engelmaier do not include a saturation effect, and Unovis/BU report an inverse linear dependence ( $1/N_F = \beta + \alpha t_d$ ) that shows no sign of leveling off up to two hours. Extrapolating this dependence to a diurnal cycle (with the same ramp rates), Unovis/BU would predict an acceleration factor of 15 times, and Engelmaier one of 1.6 times.

To make matters worse, the dwell time dependence appears to become stronger for smaller strains, including lower  $\Delta T$ , so we would expect the potential differences between predicted and actual acceleration factors to increase closer to realistic service conditions.

Finally, one major difference between an accelerated test and service is the much longer aging at elevated temperatures in the latter. Suhling et al. [39] report extreme effects of long term aging on the properties of lead free solders, and a systematic study by Unovis/BU [45] supports the relevance of those for realistic BGA joints. The properties of the solder are expected to keep changing for many years in service. The effective activation energy for this is extremely low, so experiments with a 1,000 hours@125 °C preconditioning step before thermal cycling may only represent about four months at an operating temperature of 50 °C! A significant effect on acceleration to much longer life in service cannot be excluded.

In summary, a limited number of accelerated test results already deviated from current model predictions of acceleration factors because of variations with solder joint dimensions (2.5 times) and dependence on temperature range (1.7 times) and dwell time (two times). The most unlucky combination of these **documented** deviations could already multiply up to an error of more than eight times. In addition, **documented** trends show that the errors in dwell time dependence are likely to increase further under realistic service conditions. Also, simultaneous long term aging is likely to have significant effects. Finally, extrapolation along the dwell time dependence proposed by Unovis/BU suggests the potential for further errors because of this effect alone. We therefore suggest the **likelihood** of errors up to more than half an order of magnitude (five times) for some applications and the **potential** for errors of considerably more than an order of magnitude (10 times).



# Appendix B

## CREATING A HIGH PERFORMING TEAM OF EXPERTS: A CASE STUDY OF THE LEAD FREE ELECTRONICS MANHATTAN PROJECT

Richard R. Reilly, PhD  
May 25, 2009

### Executive Summary

The Lead Free Electronics Manhattan Project – Phase I brought together leading experts in the area of lead-free electronics for a focused two-week project. The objective of the project was to develop a report that outlined baseline or best practices in lead-free electronics manufacturing. The purpose of this case study is to describe the background, planning and organization for the project, to describe some of the important aspects of the project from a process point of view, and discuss the key factors that led to the development of a high performing team, and a successful outcome.

The genesis of the project originated with the European Union RoHS directive and the associated WEEE directive, both of which have spurred commercial manufacturers to phase out the use of lead in manufacturing. This has led to a number of critical issues for aerospace, defense and other industries, as well as a high degree of uncertainty as to what practices should be used in lead-free electronics manufacturing. The project began with a vision aimed at reducing this uncertainty through a phased approach that included (1) identifying the baseline, or best practices used today, (2) developing a roadmap for R&D, and (3) conducting the R&D necessary to mitigate the problems of lead-free electronics. This vision was then translated into a series of steps that began with securing funding for the project. Once this was accomplished the SME team was selected and pre-planning for the two-week session began. The two weeks opened with a two-day Industry Forum during which outside speakers presented material on lead-free manufacturing. This was followed by a translation of the vision into more specific objectives and tasks for the teams. The team was then divided into five sub-teams focusing respectively on design, manufacturing, testing, reliability and sustainment. A structured process was followed that included detailed outlines, storyboards, a review process and final drafts. Several key factors led to the success of the project. These included clarity of vision, leadership, team selection, effective collaboration, knowledge management, a structured development process and a good technical support system. Finally, some additional lessons learned had to do with technology, selection and preparation of outside speakers, and the writing process.

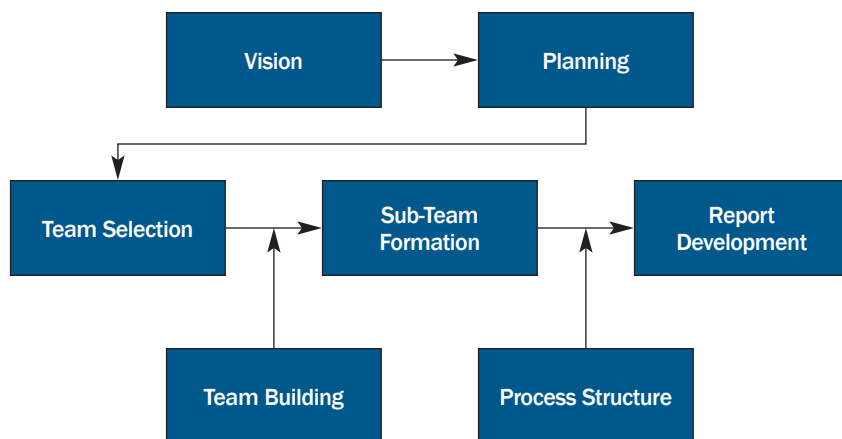
### Background

For over 50 years, manufacturers have used the eutectic alloy of 37% lead and 63% tin for soldering in electronic components. SnPb, or SnPb solder as it is commonly known, has a number of desirable properties that make it ideal for electronics manufacturing. It is easy to work with (solderability), is relatively inexpensive, has a lower melting point and creates stronger solder joints. Perhaps the most important feature of SnPb is that it essentially eliminates the growth of “tin whiskers.” Tin whiskers are tiny hairs, or whiskers, that form on tin and can lead to short circuits and metal vapor arcs. Whiskers can also break off, creating foreign debris within the component. Any one of these problems can cause the catastrophic failure of a system. Failures due to tin whiskers have been documented in commercial satellites, medical equipment, telecommunications, missile and radar systems, nuclear utilities and computers.

In February, 2003 the European Union adopted the RoHS directive. The directive banned “placing on market” new electronic equipment containing specific levels of six different substances: lead, mercury, cadmium, hexavalent chromium, polybrominated biphenyls, and polybrominated biphenyl ether. The directive went into effect in July 1, 2006. A second concurrent directive, WEEE, aimed to minimize the impact of electronic waste by encouraging and setting standards for the collection, treatment and recycling of waste. It makes the producer responsible for adverse effects. There is related legislation in China, Korea and Japan.

Currently, the U.S. has no legislation in place, but commercial manufacturers worldwide have begun transitioning to Pb-free manufacturing with the eventual phasing out of lead. A succinct statement of the current status was given in the introduction to Phase I of the Lead Free Electronics Manhattan Project (LFEMP). “The predictability of Pb-free solders in long life cycle products, using present modeling techniques, is limited due to the lack of reliable data and cannot therefore be used as a metric of future solder joint behavior. The acceleration factors – which are a key element in reliability modeling – have not yet been proven to satisfy products engaged in military and high infrastructure environments.”

The present report provides a description of Phase I of the LFEMP. The evolution of the project is summarized beginning with the vision, the selection of the team, the setting and schedule, project artifacts and project results. The factors that enabled a diverse group of experts to become a high performing team within a short time frame are then detailed.



**Figure B.1 Overview of The Lead Free Electronics Manhattan Project**

Figure B.1 shows an overview of the project flow from the development of the vision to the project outcome, and the development of the final report. The project began with a vision, planning took place over several months during which team selection occurred. Once the team was assembled, team building took place and sub-teams were formed. A structured process enabled sub-teams to quickly focus on their task and to develop the final report.

### Developing the Vision for LFEMP

Much of the success of Phase I of the LFEMP project can be attributed to the development of a clear vision. The development of this vision began in 2004 when the Lead Free Electronics in Aerospace Project Working Group (LEAP-WG) was formed to provide input into standards and industry guidelines. LEAP holds meetings several times a year and it was at one of these meetings in Ulm, Germany that Dave Humphrey found himself sitting next to Ed Morris.<sup>1</sup> In a side conversation Dave said, “wouldn’t it be great if we could do something about the lead-free problem?” Dave remembers that the conversation led to further discussions, which then led to the idea that what was needed was a highly focused project that would bring together the leading experts in Pb-free electronics to identify current best practices, develop a roadmap for what needs to be done to address the challenges of Pb-free electronics, and carry out the necessary research and development. Thus, the initial vision of the Lead Free Electronics Manhattan Project was formed. In 2008, the Industry Advisory Board (IAB) and the ONR were briefed on these plans and suggested a phased approach. Phase I would focus on current baseline practices and would identify best practices where they existed. Phase II would focus on developing the roadmap for the work that needs to be done in research and development. Phase III would be a three-year effort aimed at conducting the R&D necessary to develop reliable and predictable Pb-free electronics.

<sup>1</sup>A list of the affiliations of all key experts involved in the LFEMP is provided in Appendix C.

The initial vision for the first two phases was stated as follows:

*The objective of this effort is to capture industry-wide Pb-free electronics best practices and to develop an integrated industry/government plan to mitigate future risks posed by the worldwide transition to Pb-free electronic products. The scope of this effort will be to assemble leading subject matter experts and have them collectively define the current set of best practices in use to mitigate the risks associated with Pb-free electronics usage in DoD applications and then to develop an action plan to mitigate future risks.*

### Pre-Project Planning

Pre-project planning began in February of 2009 with a teleconference that included the conference coordinator, the two co-leaders, and the facilitator. It was determined that the LFEMP would be a two-week, intense effort that would bring together a group of the leading Pb-free SMEs to one location. Teleconferences were held every two weeks until the project started. Topics covered in these meetings included logistics for the conference, outside speakers, the work structure, the facilitation process and the desired outputs. Drafts of a possible structure and schedule were circulated and commented upon and there was an eventual consensus as to how the two weeks would be structured, a detailed schedule, how the work flow would be managed, how issues related to team process would be handled and what the outputs would be.

### Team Selection

A critical step in the process was the selection of the team of SMEs who were to participate in the two-week session. The primary objective of the team selection process was to identify individuals with the best combination of experience, knowledge and expertise in lead-free electronics who might serve as team members for the LFEMP. Two operational constraints were added. The first was that the group should broadly represent the Aerospace Industry and DoD service organizations. A second constraint was that the group should be limited to 15 participants.

The selection of the team began with one of the co-leaders identifying four well-known experts in Pb-free electronics to serve as an advisory panel. Through emails and teleconferences, the advisory panel identified a group of peers with the requisite qualifications. The advisory panel then did a preliminary ranking of the identified individuals. At this point, the members of IAB and seven director-level representatives from industry were asked to review the list and add/subtract names. Once this list was developed, the IAB and the advisory panel re-ranked the names in a spreadsheet. The ranks from each individual were sent to the co-leader who aggregated all of the rankings by taking the average rank across all SMEs and IAB members. A consolidated list of 37 SMEs was prepared and sent back to the IAB for review. Individuals were invited to participate in the LFEMP according to their overall ranking. If an individual could not participate for any reason, the next-ranked name on the list was invited until a total of 15 SMEs had agreed to participate. Although other industry

representatives offered to fund the participation of additional SMEs, the group size remained at the 15 selected by this process. It was decided that having a representative from the military was important, so an additional SME from the Army (AMRDEC) was asked to join the group. An SME from ACI Technologies, Inc. (ACI) also served in the group, bringing the total count to 17.

## **The Setting and Schedule**

### *Setting*

The two-week session was held at the headquarters of ACI in Philadelphia. The full team met in a large conference room with an audio-visual set-up that included a projector and teleconference equipment. Since the larger group was organized into five sub-teams, five separate breakout rooms were also provided. For the full-team sessions, audio recordings were made via individual microphones assigned to each of the SMEs. In addition, selected video recordings were made during the two weeks.

### *Schedule*

Each day of the two weeks began at 8am. The “tag-up” session at the end of every day was an important feature. These sessions were intended to review outstanding issues, problems, questions and lessons learned. Key points were recorded on an easel and posted in the large conference room.

- **Day 1**  
The project began with a welcome from the B2PCOE Director and a presentation from the Director of Navy ManTech Program. The co-leaders provided an overview of the schedule, the project purpose and vision. The notion of best practices was introduced, discussed and a consensus was arrived at for a definition of best practices in Pb-Free electronics. Afterwards, the Industry Pb-Free Electronics Best Practices Forum began. The forum included presentations on varied issues from experts in Pb-free electronics. Most of the presentations were made via teleconferencing using speakerphone and a web conferencing platform. Questions and discussions were typically integrated into the sessions.
- **Day 2**  
The Industry Pb-Free Electronics Best Practices Forum continued.
- **Day 3**  
The full team engaged in a more general discussion of the lessons learned from the outside speakers. Additional presentations were made by members of the team and the team discussed lessons learned.

## Appendix B

---

- **Day 4**  
The co-leaders and the team discussed the deliverable and refined the outline for the final reports. Individual SMEs were assigned to five specific teams with responsibility for developing reports in the following areas: Design, Manufacturing, Testing, Reliability and Sustainment. A preliminary outline was provided for each report (included at the end of this section). Leaders for each team were assigned. Each team included three SMEs, with the exception of Manufacturing, which had four SMEs. Teams began working in their respective breakout rooms. As a first step, each team refined their initial outline for the deliverable. Outlines were posted on the wall and sub-team leads discussed the outlines and received feedback from the LFEMP co-leaders and other SMEs.
- **Day 5**  
Teams continued refining outlines and began developing initial storyboards. Working continued off-line, over the weekend to refine their storyboards.
- **Day 6**  
Teams developed an initial set of storyboards and posted them on the wall. Sub-team leads gave an overview of their storyboards, SMEs commented and gave feedback.
- **Day 7**  
Teams began writing their draft sections. Written material was posted and made available for feedback by SMEs using post-it notes or in the general session.
- **Day 8**  
Writing continued as on the previous day.
- **Day 9**  
Sub-teams continued writing as on the previous two days.
- **Day 10**  
Teams completed their initial drafts and agreed on follow-up activities over the next two weeks. Follow-up activities included completing drafts, editing and feedback on final drafts for the report. The two-week session ended with a recognition event and awarding of certificates to all SMEs.

### Development of Team Norms and Project Culture

One of the important features that contributed to the success of the LFEMP was an early development of norms. A session was held with the entire team to solicit their input on a “code of conduct” for the two weeks. For purposes of discussion, the code of conduct was organized around four categories of team behavior: communication, conflict management, self-management and process review.

### *Communication*

The team agreed on the following principles.

- All team members listen attentively to other speakers and allow them to finish before commencing.
- If a team member wants to speak, he or she must raise their hand and be recognized.
- Team members will avoid dominating discussions and allow everyone to share in the conversation. A three-minute rule was suggested; e.g., any single speaker who speaks over three minutes will be stopped.

### *Conflict Management*

The team agreed on the following ground rules for managing conflict.

- Ok to agree to disagree respectfully
- Respect minority opinions
- Don't avoid tough issues/questions
- Goal in discussions is to arrive at a win-win resolution
- In the final analysis, debates should be settled by data where possible ("data talks")

### *Self-Management*

The following rules were agreed upon for self-management of the LFEMP team.

- Three-knock rule: when the team or discussion got off point or involved side conversations, the co-leaders or any member could knock three times as a signal that the group should be quiet and listen to the speaker.
- Three-minute soap box rule: no speaker should be allowed to speak more than three minutes.
- Necessary and sufficient: discussions should last no longer than that which is necessary and sufficient to cover the points.
- Content over volume: the content of discussions should be emphasized over the volume of the speech.
- There should be a scribe for each session to record key points and issues for feedback and review.
- Issues that cannot be addressed immediately should be captured in a "parking lot."

## Appendix B

---

### Process Review

- End-of-day tag-up sessions can be used to review any team process issues.
- If the process is not working, fix it immediately.

### Artifacts

The LFEMP culture was characterized by several artifacts that helped to keep the team focused on their end objectives. Artifacts included a professionally done brochure, LFEMP storyboards (see Template at the end of this section), and a baseball bat.

The brochure included an overview of the project and outlined the schedule and agenda. Biographical information on each SME was also presented in the brochure.

The storyboards provided a structure for the sub-team to assemble their initial ideas and share them with the other SMEs. Storyboards included the following sections: A heading for the module, identifying information for the authors, references, conclusions, recommendations, the current baseline practice, issues/gaps/misconceptions and a space for figures, charts or pictures with captions. As storyboards were prepared, they were posted on the wall under the relevant topic and other SMEs could review and post comments.

The baseball bat was a humorous symbol used to “enforce” the ground rules, and to keep the SMEs on track for the primary objective.

### Benchmarking and Best Practices Review

Early in the project, material related to benchmarking and best practices was reviewed. Standard definitions were presented for best practices; however, after a thorough discussion, the SME team reached a consensus that the term “best practice” did not apply to many areas that were being addressed in the LFEMP. Many of these issues lacked sufficient data and experience to make a determination as to whether a practice was best or not. An alternative definition was agreed to as follows: *A process or practice that describes the current state-of-the-art as a baseline against which future improvement can be measured.* It was also agreed upon that if a baseline practice was a best practice, it would be so identified.

### Project Outcome

Overall, the LFEMP team functioned extremely well and was successful in meeting the objectives. Although the schedule was demanding and the task was difficult, the sub-teams were all able to produce first drafts by the end of the two week period. Even though follow-up work was needed to turn the drafts into a final report, the majority of the work was completed within the two weeks.



## **The Keys to Success**

The successful outcome of the LFEMP was made possible by seven factors that characterize high performing teams.<sup>2</sup> These included clarity of vision, leadership, team selection, knowledge management, effective collaboration, a structured development process and a good technical support system.

### *Clarity of Vision*

The vision for the project was clear and more importantly, it was communicated to all team members in several ways. First, the written material sent in advance to team members, outlined the objectives of the project. As the team met over the first few days, the vision was discussed, refined and agreed upon by the entire team. The team had a common understanding of the vision and was able to achieve what team researchers call a “shared mental model,”<sup>3</sup> This allowed the team to see the entire vision for the project and how each of the elements fit together interdependently. This shared mental model was enhanced by frequent feedback from the co-leaders and fellow SMEs as the project progressed. A good example of how the shared mental model was expressed was in the agreement of the teams to use a common set of colors for visuals: green for no change, yellow for minor change and red for major change.

### *Leadership*

The two co-leaders contributed to the ultimate success of the project in several important ways. First, they set the vision for the end-product and continually clarified and reinforced the vision so that all team members developed a shared mental model. Secondly, the co-leaders kept the team on task by providing feedback on the schedule and the content of each sub-teams’ contributions. Third, the co-leaders participated fully in the process, leading review sessions, contributing knowledge and expertise, helping to integrate the various elements provided by sub-teams and writing sections of the report. Finally, the co-leaders motivated the team through their encouragement, obvious commitment and exemplary behavior.

### *Team Selection*

The LFEMP recruited the “A Team” – a group of the top experts on Pb-free electronics. The process used to select these individuals was systematic and incorporated the judgment of a sizable group of knowledgeable, senior managers and leaders in the field of electronics. In addition to bringing their experience, knowledge and expertise, team members – without exception – also brought a passion and commitment to the issue of Pb-free electronics manufacturing. This combination of expertise and commitment was an essential combination for success. There was also a social

---

<sup>2</sup>Lynn, G., Reilly, R. (2002). *Blockbusters: Developing Award-Winning New Products*. Harper-Collins.

<sup>3</sup>Mathieu, J., Heffner, T., Goodwin, G., Cannon-Bowers, J., Salas, E. (2005). Scaling the quality of teammates’ mental models: Equifinality and normative comparisons. *Journal of Organizational Behavior*, 26, 37-56.

networking element to the team's effectiveness. Previously-established relationships with one another through professional groups and meetings allowed team members to move quickly past the initial stages of team development and begin working together effectively and quickly. Social networking with experts outside of the team also allowed information to be obtained and assimilated through the outside speakers and "lifelines" that could be called upon for information or advice on specific key issues.

### *Knowledge Management*

The LFEMP was a complex undertaking with a large amount of knowledge and data to be presented, discussed and assimilated. The effective management of knowledge during the two weeks was accomplished in several ways.

- **Outside Presentations and Review**  
Industry forum presenters were selected to provide useful, and in some cases, provocative information for the SMEs. Each day wrapped up with a review session to discuss the presentations and highlight what one of the co-leaders called "aha" or "hmm" reactions. Were there insights or thought-provoking aspects of a particular presentation that might have implications for Pb-free electronics manufacturing? These follow-up sessions were lively and gave SMEs an opportunity to discuss their own views and thoughts on the same topic, to indicate that something new had been learned or to agree that much more data was needed.
- **Tag-up Sessions**  
Tag-up sessions were held at the end of each day to review progress, outstanding issues, team process issues, scheduling issues and any other topics that might come up. These sessions often included the exchange of information or a discussion of process issues that helped all SMEs to stay on schedule and understand the perspective that other sub-teams were taking with respect to particular issues.
- **Tacit Knowledge Exchange**  
Much of the knowledge about Pb-free is not codified, but resides with SMEs. This tacit knowledge was exchanged through industry forum presentations, SME team discussions, and discussions within and between sub-teams.
- **Storyboarding and Posting**  
Storyboards provided a concise way of presenting information and allowing the review and comments of all SMEs. Once storyboards were completed, actual text and visual material was posted. Reviews and comments allowed all SMEs to track the progress of each sub-team.

- **Co-Leader Review and Feedback**

The co-leaders provided continual feedback during the two weeks, added additional thoughts and information. Co-leaders were able to take a broader perspective by reviewing the progress of all sub-teams and providing feedback to both sub-teams and the full SME team in general sessions.

### *Effective Collaboration*

The larger team was able to collaborate effectively in the early stages of the project by adhering to the code of conduct and engaging in constructive conflict. Ground rules were generally followed with occasional reminders about hand-raising and use of the three-knock rule. Sub-teams also functioned effectively and met with one another to discuss interdependencies and ensure that issues were being handled consistently. Conflict during the sessions was always about the task or the process and never about individuals. As one of the SMEs remarked on the last day of the project, “nobody’s ego got in the way and nobody came with an agenda.” The sub-teams interfaced effectively and helped one another when it was appropriate, even writing specific sections for another sub-team in some cases. One important feature of the LFEMP was the co-location for two-weeks of all team members. This provided fertile ground for the exchange of tacit knowledge between team members that would have been otherwise difficult or impossible without the collocation. The use of outlines and storyboarding promoted collaboration as it allowed all sub-teams to understand what was being covered, where there might be overlap, where there were inconsistencies, where there might be a need for cross-team collaboration and where there might be gaps in what was covered. In addition, most team members were housed in the same hotel, allowing off-line discussions and relationship-building that helped the team to continue to work together effectively. This was further enhanced by two nighttime team-building activities (a major league baseball game and a dinner cruise) during which the team was able to relax and share some fun time together.

### *Structured Development Process*

A final key to the success of the LFEMP was a structured development process. The process began with a template for the reports which were then turned into outlines by the sub-teams. Following the development and review of outlines, the sub-teams prepared storyboards which addressed specific elements of their report. Finally, storyboards were turned into draft reports. As noted, an important element of the process was the posting of material at each step. This allowed feedback, coordination, identification of overlap or other issues that needed to be addressed and made the eventual report writing easier. One other element of the process that should be mentioned is a hard deadline for completing the drafts imposed by the co-leaders with a well-defined schedule. The deadline served to mobilize and focus the efforts of the team and made keeping on schedule essential. Specific milestones were used by sub-teams and the co-leaders to monitor progress.

### *Technical Support System*

Supporting technology was used to help the team achieve its goals in several ways. First, most outside speakers were not on-site, so web-enabling technology and teleconferencing equipment was used to allow speakers to present information and dialogue with the LFEMP SMEs. Second, all SMEs had access to the internet which allowed them to search for information and communicate via email to other experts. A local FTP site was established so that sub-teams, co-leaders and individuals could both upload and download documents as they were prepared. In addition, resource materials were uploaded and resided on the FTP site for easy access by SMEs at any time. Breakout rooms had a projector and wireless connections so that sub-teams could share focus on material as it was being developed.

### **Some Additional Lessons Learned**

The LFEMP was an unusual project in several respects. It brought together leading experts in a specific area of technology, used a structured processes and resulted in an end-product in a short timeframe. Although the project was successful and could be considered a best practice in organizing and implementing a focused undertaking with SMEs, there were additional lessons learned that may be useful for future projects of this type.

#### *Preparation and Application of Technology*

- Web-based technology allowed outside speakers from all over the U.S. to present material relevant to Pb-free electronics. The ease with which both speakers and the on-site SMEs were able to utilize the technology was variable, however. An easy to use platform that allows speakers more readily control and present their material, while also providing clear audio for easy discussions, would be a valuable asset.
- A dedicated server that could be utilized as a repository for all resources and documents for the project would also be invaluable. This allows all SMEs to upload and download documents quickly. Again, making the technology simple and easy to use is important.
- All breakout rooms should have projectors, good wireless connections with access to the server, the internet and printers.

#### *Outside Speakers*

- Speakers need to be focused and crisp in their presentations. A common format for outside speakers should be developed with time for presentation and discussion.
- SMEs, if possible, should review speakers and their planned presentations for relevance to the topic at hand.

### *Report Preparation*

- Not all presenters were comfortable writing in the breakout rooms. If possible, separate private space could be provided for SMEs who need a quiet space to write effectively.
- Issues such as formatting, spacing, fonts, treatment of acronyms and how graphs, pictures and figures are handled should ideally be decided upon ahead of time.
- To the extent possible, SMEs should know the specific areas of focus about which they will be writing. This would allow them to bring relevant materials, reports, etc., with them.

### **Conclusions**

The LFEMP is an example of a project that could be replicated for other technical areas. As such, it represents a good example of a best practice for bringing together experts to focus on a problem and produce a useful outcome in a short time frame. It is suggested that the seven principles described here – clarity of vision, leadership, team selection, knowledge management, effective collaboration, a structured development process and a good technical support system – should be followed to ensure a high performing team and a successful project outcome.

## **OUTLINE FOR LFEMP REPORTS**

Executive Summary (1 page)

Table of Contents

Exhibits

List of Figures, Graphs, Tables

I Introduction (1 page)

II Pb-Free Electronics Overview (2 pages)

III Risk Associated with Pb-Free Electronics Applications in Aerospace/Military Products (3 pages)

IV Best Practices Section

A. Printed Wiring Boards

1. Product Design and Development

i. Best Practices Summary

ii. Current Issues/Roadblocks with Best Practices

iii. Conclusions

iv. Recommendations

2. Pb-Free Electronics Manufacturing
  - i. Best Practices Summary
  - ii. Current Issues/Roadblocks with Best Practices
  - iii. Conclusions
  - iv. Recommendations
3. Verification, Validation, and Qualification Best Practices Testing
  - i. Best Practices Summary
  - ii. Current Issues/Roadblocks with Best Practices
  - iii. Conclusions
  - iv. Recommendations
4. Product Sustainment
  - i. Best Practices Summary
  - ii. Current Issues/Roadblocks with Best Practices
  - iii. Conclusions
  - iv. Recommendations

### B. Solder Attachments

1. Product Design and Development
  - i. Best Practices Summary
  - ii. Current Issues/Roadblocks with Best Practices
  - iii. Conclusions
  - iv. Recommendations
2. Pb-Free Electronics Manufacturing
  - i. Best Practices Summary
  - ii. Current Issues/Roadblocks with Best Practices
  - iii. Conclusions
  - iv. Recommendations
3. Verification, Validation, and Qualification Best Practices Testing
  - i. Best Practices Summary
  - ii. Current Issues/Roadblocks with Best Practices
  - iii. Conclusions
  - iv. Recommendations
4. Product Sustainment
  - i. Best Practices Summary
  - ii. Current Issues/Roadblocks with Best Practices
  - iii. Conclusions
  - iv. Recommendations

- C. Component and Lead Finishes
  - 1. Product Design and Development
    - i. Best Practices Summary
    - ii. Current Issues/Roadblocks with Best Practices
    - iii. Conclusions
    - iv. Recommendations
  - 2. Pb-Free Electronics Manufacturing
    - i. Best Practices Summary
    - ii. Current Issues/Roadblocks with Best Practices
    - iii. Conclusions
    - iv. Recommendations
  - 3. Verification, Validation, and Qualification Best Practices Testing
    - i. Best Practices Summary
    - ii. Current Issues/Roadblocks with Best Practices
    - iii. Conclusions
    - iv. Recommendations
  - 4. Product Sustainment
    - i. Best Practices Summary
    - ii. Current Issues/Roadblocks with Best Practices
    - iii. Conclusions
    - iv. Recommendations
- D. Mechanical Parts
  - 1. Product Design and Development
    - i. Best Practices Summary
    - ii. Current Issues/Roadblocks with Best Practices
    - iii. Conclusions
    - iv. Recommendations
  - 2. Pb-Free Electronics Manufacturing
    - i. Best Practices Summary
    - ii. Current Issues/Roadblocks with Best Practices
    - iii. Conclusions
    - iv. Recommendations

### 3. Verification, Validation, and Qualification Best Practices Testing

- i. Best Practices Summary
- ii. Current Issues/Roadblocks with Best Practices
- iii. Conclusions
- iv. Recommendations

### 4. Product Sustainment

- i. Best Practices Summary
- ii. Current Issues/Roadblocks with Best Practices
- iii. Conclusions
- iv. Recommendations

### V Pb-Free Electronics Reliability (10 pages)

- A. Modeling and Tools
- B. Predicting MTBF and Availability

### VI Conclusions (3 pages)

### VII Recommendations (2 pages)

Exhibits

## LFEMP STORYBOARD TEMPLATE

*(see next page)*



## Storyboard Outline Form

Section or Subsection:	Author:
Module Number and Title:	References:
Date:	Phone:
<p>Conclusions:</p> <hr/> <hr/>	
<p>Recommendations:</p> <hr/> <hr/>	
<p>Current Baseline Practice:</p> <hr/> <hr/> <hr/> <hr/>	<hr/> <p>Two-Part Caption:</p> <hr/> <hr/>
<p>Issues/Gaps/Misconceptions:</p> <hr/> <hr/> <hr/> <hr/>	

# Appendix C

## BIOGRAPHIES

### **Dr. Joseph P. Lawrence, III    Special Guest**

*Director of Transition, Office of Naval Research*

Joseph P. Lawrence, III, received a B.S.E.E. from the University of Maryland, College Park, an M.S.E. from Princeton University, and a Ph.D. from the University of Maryland, College Park, all in Electrical Engineering.

Dr. Lawrence started his career as a member of the technical staff at the Naval Research Laboratory in Washington, D.C., in 1966, initially with the Radar Division, working on a variety of radar and multi-sensor integration projects. He later joined the NRL Tactical Electronic Warfare (EW) Division, where he was responsible for anti-ship missile engagement modeling development and applications, as well as a large variety of EW systems analysis, development, and evaluation efforts as Head of the Advanced EW Systems Section. Subsequently, as Head of the Surface EW Systems Branch, he was responsible for research and development of systems and techniques spanning the full timeline of surface EW engagement.

Dr. Lawrence was selected to be the ONR Manager for the Fleet/Force Protection Future Naval Capability (FNC) initiative in 2000, where he was responsible for a wide range of applied S&T including platform signatures, sensors, HM&E, and defensive weapons. He was appointed as the Director of the ONR Surveillance, Communications and Electronic Combat Division (ONR 313) in September 2001. In this latter position, he was responsible for performance of DoN S&T in the areas of surveillance (RF and EO/IR), communications, navigation (including GPS), and electronic warfare.

In 2004 he was detailed as Associate Technical Director – Transitions (ATD-T) for the Office of Naval Research, and as such has responsibility within ONR for approximately one third of the DoN S&T budget, including FNCs and ACTDs.

In 2005 he was formally selected as the ATD-T, which has since been re-titled as the Director of Transitions. He is a member of the Federal Senior Executive Service.

**John Carney    Special Guest**

Mr. John Carney heads the Navy Manufacturing Technology Program (ManTech) at the Office of Naval Research. ManTech is an industrial preparedness program focused on developing the process technology needed for industry to produce Navy weapon systems. It provides a crucial link between technology invention and industrial applications by maturing and validating emerging manufacturing technologies to support implementation in industry and DoD facilities. The program is currently aimed at improving shipbuilding affordability.

Mr. Carney began his Navy career in the Shipbuilding Technologies Division of the David Taylor Research Center, now the Naval Surface Warfare Center, Carderock Division. He joined the Office of Naval Research in 1998 and served as program manager for several of ManTech's Centers of Excellence and as ONR's liaison to the National Shipbuilding Research Program prior to becoming the ManTech Director.

His education includes a B.S. in Industrial Engineering and Operations Research and Masters of Engineering Administration, both from Virginia Tech.

**Rebecca D. Clayton    Special Guest**

Mrs. Clayton is currently a GS-15 assigned to the Office of Naval Research, ManTech as the Program Officer for the Navy Joining Center and the Benchmarking and Best Practices Centers of Excellence.

Clayton left industry in 1999 to begin her career with the DoD working for the U.S. Army in the Fire Support Armaments Center (FSAC) at Picatinny Arsenal. Here she served as the Test Director and Project Manager for several guided munitions programs, Executive Officer to the FSAC Commander and SES for Technology, and Chief Operations Officer for OPM CAS. In 2004, she reported onboard the USMC; Joint Non Lethal Weapons Directorate, Quantico, Virginia; to direct the joint-service/interagency efforts on the Radio Frequency Directed Energy Vehicle/Vessel Stopper Technology Investment Program. In November 2004, Mrs. Clayton was recruited to become the Test Missile Reentry Body and Systems Instrumentation Engineer at Strategic Systems Programs, U.S. Navy in support of the U.S./U.K. Test Missile, RB, instrumentation, test and evaluation, acquisition, and operations. In 2006, she checked into the Pentagon to serve as the Principal Advisor for the Chief of Naval Operations (CNO), OPNAV N80, for all matters relating to Irregular Warfare, Expeditionary Warfare, and Global War on Terrorism (GWOT).

She is a graduate of the New Jersey Institute of Technology with Bachelor of Science and Master of Science Degrees in Mechanical Engineering, and is presently pursuing her Ph.D. in Technology Management from Stevens Institute of Technology. She is married to Captain Edmund G. Clayton, Ph.D., USMC.

### **Gerald Aschoff**

Gerald (Jerry) Aschoff is presently a Program Manager for development of Special Projects within Integrated Defense Systems business in The Boeing Corporation. He is currently headquartered in Huntington Beach, CA. Jerry has also managed the research engineering department as well as serving as the Director of Operations and Technology at Boeing. He has extensive experience in the areas of systems engineering, research and development, systems analysis and requirements, process development and improvements, technology development, team development and project management. His technical area of expertise is in electromagnetic propagation and subsequent systems analysis and effects. He continues to be active as a leader for the Industrial Advisory Board, and various other councils and consortiums both within and outside of Boeing.

His educational background includes an MA (Magna Cum Laude) in Mathematics from California State University, and has taught the calculus and higher level math courses at Concordia University and Rancho Santiago College. He also holds Executive MBA certificates from the University of Washington (2001) and Stanford University (2006).

### **Peter Borgesen**

Peter Borgesen has a Ph.D. in Physics from the University of Aarhus in Denmark. He worked at national laboratories there and in Germany, as well as in the Materials Science Department at Cornell University, before joining the SMT Laboratory at Universal Instruments Corporation in 1994. In 2006, this laboratory and other parts of Universal were combined to form a separate division, Unovis Solutions. Peter is the manager of the AREA Consortium which sponsors a multi million dollar research effort by the laboratory on automated first and second level microelectronics assembly processes and reliability. A major emphasis of this research is on lead-free issues. He is also a professor of Systems Science & Industrial Engineering at Binghamton University.

### **Lloyd Condra**

Lloyd Condra is a Technical Fellow in the Boeing Research and Technology organization in Seattle, WA. Mr. Condra is the founding Chairman of the Lead-Free Electronics in Aerospace Project (LEAP), which is sponsored jointly by the Aerospace Industries Association (AIA), the Avionics Maintenance Conference (AMC), and the Government Electronics and Information Technology Association (GEIA). LEAP is the largest military/aerospace activity devoted to responding to the challenges posed by the global transition to lead-free electronics. LEAP includes representatives from every major entity in the aerospace industry around the world, and it has published standards and policy recommendations in use throughout the military and aerospace industry.

Mr. Condra also is chairman of International Electrotechnical Commission Technical Committee 107 (TC 107), Process Management for Avionics. TC 107 includes 20 member countries, and is the international publication organization for the LEAP-WG lead-free documents and numerous other avionics standards. He is also chairman of the GEIA Avionics Process Management Committee, which publishes the lead-free and other avionics documents in the U.S. He has authored over 50 technical papers on electronics assembly and reliability, and three technical books. He is a senior member of IEEE. He holds a B.S. from Iowa State, and an M.S. from Lehigh, both in materials engineering.

### **Carol Handwerker**

Carol Handwerker is a Professor of Materials Engineering, at Purdue University, West Lafayette. Prior to joining Purdue in August 2005, Dr. Handwerker served as Chief of the Metallurgy Division at NIST for the last nine of her 21 years at NBS/NIST. In her role as Division Chief, she led a staff of approximately 80 scientists and administrative staff members (~40 full-time government employees and 40 guest scientists, research associates and contractors) in technical programs aimed at developing the materials measurement and standards infrastructure important to U.S. industrial competitiveness and infrastructure protection. In addition to her role as NIST Metallurgy Division Chief, she assisted the U.S. microelectronics industry in the worldwide conversion to lead-free solders for printed wiring boards by developing the link between many fundamental science concepts and high volume electronics manufacturing. She co-chaired the Alloy Development team in the NCMS Pb-Free Solder Consortium (1994-1997) and the iNEMI Alloy Selection Group (1999-2002), within the iNEMI Pb-Free Assembly Project, the major U.S. industrial consortium responsible for conversion to lead-free solders in printed wiring boards and components. Dr. Handwerker's research program at Purdue is focused on Pb-free interconnects, particularly for high reliability server, military, and aerospace electronic systems, on innovative processing strategies for next-generation electronic packaging, and on including sustainability in the design of new electronic materials, processes, and products. Her research team at Purdue is part of the NSWC Crane/SAIC Program on the Logistics Impact of Lead-Free Components on Legacy Electronic Repair, the HDPUG project on Microvoid Formation in Solder Interconnects, the iNEMI Tin Whisker Formation Project, and the AFRL project on Solderless Interconnects with Nanodynamics, Heraeus, and MacDermid.

### **Craig Hillman**

Craig Hillman, Ph.D., CEO and managing partner of DfR Solutions, is an expert in the development and implementation of strategic reliability processes and operations. His specialties include best practices in Design for Reliability (DfR), strategies for transition to Pb-free, supplier qualification, accelerated test plan development, and root-cause analysis of component, interconnect, and printed board failures. Dr. Hillman has over 45 publications and has presented on a wide variety of quality and reliability issues to over 250 companies and organizations, including Apple, Dell, Hewlett Packard, Motorola, IBM, Cisco Systems, General Electric, Emerson Electric, Lockheed Martin, Northrop Grumman, Raytheon, Honeywell, and General Dynamics. Over the past four years, Dr. Hillman has led DfR Solutions through tremendous growth into one of the largest and best-known reliability organizations in the international electronics marketplace. His educational background includes a post doctoral fellowship from Cambridge University, a Ph.D. in materials from the University of California, Santa Barbara, and a B.S. in metallurgical engineering and material science from Carnegie Mellon University.

### **David D. Hillman**

David D. Hillman is a Metallurgical Engineer in the Advanced Operations Engineering Department of Rockwell Collins Inc. in Cedar Rapids, Iowa. Mr. Hillman graduated from Iowa State University with a B.S. (1984) and M.S. (2001) in Material Science & Engineering. In his present assignment he serves as a consultant to manufacturing on material and processing problems. He has published 163 industry papers with the 1997 ISHM Conference paper being selected as "Best Paper of Session," the 2006 SMTAI Conference paper, the 2007 SMTAI Conference paper, and the 2008 SMTA International Conference on Soldering & Reliability being selected as "Best of Conference." He has presented 11 Electronics Industry tutorials. Mr. Hillman was awarded the Da Vinci medal as a Rockwell Engineer of the Year for 1994. He serves as the Chairman of the IPC JSTD-002 and -003 Solderability committees. Mr. Hillman served as a Metallurgical Engineer at the Convair Division of General Dynamics with responsibility in material testing and failure analysis prior to joining Rockwell. He serves as a member of the SMTA Journal and Soldering & Surface Mount Technology Journal Technical Paper Review committee. He is a member of the American Society for Metals (ASM), the Minerals, Metals & Materials Society (TMS), and Surface Mount Technology Association (SMTA) and the Institute for Interconnecting and Packaging of Electronic Circuits (IPC).

### **David L. Humphrey**

David L. Humphrey is a Senior Principal Engineer at Honeywell with over 20 years in aerospace and is currently on staff at Honeywell International in materials and process engineering. Dave currently serves on the ECCB board of directors for IECQ, is the U.S. TA alternate on TC107 of the IEC and vice chair of the GEIA APMC, avionics process management committee. He is the Honeywell technical

POC for several AVSI, Air Vehicle Systems Institute, research projects, the Honeywell Aerospace sector membership in the CALCE research consortium at the University of Maryland and is on the planning team for a potential major modernization assessment of reliability systems tools for the aerospace industry and US Military. Previously he worked for 12 years in the automotive industry as a design engineer, and was the quality manager in a start-up assembly plant for General Motors in Arizona. He reviews technical books previous to publication, has been a contributing author to several standards and articles for IEEE and SAE. He has recently taught reliability methods in China. Dave is now working on GEIA standards for the aerospace industry lead-free transition.

### **David Locker**

David Locker has worked as a components engineer since 1987 with the U.S. Army, working on missile and aviation systems. He received the B.S. degree in Applied Physics and the M.S. degree (Electrical Engineering) from Georgia Institute of Technology.

### **Carmine Meola**

Carmine Meola is presently an R&D Project Manager as well as the former Manufacturing Manager of the Demonstration Factory and the Training Center at ACI Technologies, Inc. Mr. Meola has an extensive background in electronic materials, substrate processing, plating, and packaging in the PCB and semi-conductor industry. He has also leveraged his experience as a certified ISO-9001 internal auditor, and applied it in both the electronic and pharmaceutical industry. His activities led to patents for anisotropic conductive adhesives, WLBI conductive interposer, and EMI conductive foams. Mr. Meola was involved in two start-up plants, and was responsible for facilitating design, procuring equipment, and process implementation for both manufacturing and laboratory.

### **Stephan J. Meschter**

Dr. Meschter is a Senior Mechanical Engineer at BAE Systems in Johnson City, New York who has specialized in electronics packaging and failure analysis for nearly 25 years. Dr. Meschter is the company's lead-free electronics technical focal point and has been coordinating a significant portion of the company's lead-free research. He is actively participating in the AIA Lead-Free Electronics in Aerospace Project – Working Group (AIA LEAP-WG), is leading the GEIA-HB-0005-2 technical guidelines handbook and helped develop the GEIA-STD-0005-2 tin whisker risk mitigation standard and the GEIA-STD-0005-3 test protocol standard. His electronics packaging experience is primarily with power, flight and high vibration engine control electronic systems used in space, aircraft and ground vehicles. He is also participating in the JCAA/JGPP and NASA DoD lead-free consortiums where he supported the BAE Systems Irving, Texas group as they fabricated over 400 assemblies used in the JCAA/JG-PP and NASA/DoD consortium testing.

### Ed Morris

Ed Morris is currently the Director of Hardware and Manufacturing on the Lockheed Martin Corporate Engineering & Technology team. Reporting to the Vice President of Engineering, Ed works with the Lockheed Martin Business Areas to develop technical excellence, as well as a sound strategy for the hardware design and manufacturing communities across the Corporation. His focus is on improving the effectiveness of hardware design processes and methods as they influence the affordability, producibility, and testability of Lockheed Martin's portfolio of products and program execution. He is Vice Chairman of the Lockheed Martin Corporate Production Council. Additionally, Ed is responsible for developing and executing a proactive Lockheed Martin approach for Pb-free electronics.

Ed has a B.S. Degree in Aeronautical Engineering from Purdue University and an MBA from the University of Texas at Arlington. He has 37 years of defense, commercial and international aerospace industry experience with emphasis on program management, engineering, procurement, and manufacturing. Ed is a nationally recognized leader in advanced manufacturing technology.

### Michael Osterman

Michael Osterman (Ph.D., University of Maryland, 1991) is a Senior Research Scientist and the director of the CALCE Electronic Products and System Consortium at the University of Maryland. He heads the development of simulation assisted reliability assessment software for CALCE and simulation approaches for estimating time to failure of electronic hardware under test and field conditions. Dr. Osterman is one of the principle researchers in the CALCE effort to develop simulation models for failure of Pb-free solders. In addition, he has lead CALCE in the study of tin whiskers since 2002 and has authored several articles related to the tin whisker phenomenon. Further, he has written eight book chapters and numerous articles, including the Best Session Paper Award in 41st International Symposium on Microelectronics, IMAPS 2008 and the Best Paper-Maurice Simpson Technical Editors Award in the Institute of Environmental Sciences, 2008. In 2008, a Ph.D. student working under Dr. Osterman won the co-sponsored SMTA and Circuits Assembly Charles Hutchins Educational Grant for work on BGA reballing. In 2008, Dr. Osterman setup an electroplating facility for conducting tin whisker research, a vibration test facility, and initiated a pilot study on influence of charging cycle on life of rechargeable single cell and multiple cell battery packages. He has conducted multiple experiments on temperature cycling, vibration, and mechanical bend of electronic assemblies. He is a member of ASME, IEEE and SMTA.

### David Pinsky

David Pinsky is an Engineering Fellow with the Raytheon Integrated Defense Systems Mechanical Engineering Directorate. David has over 25 years experience in failure analysis and materials selection for aerospace products. He chairs the Raytheon RoHS Technical Steering Committee, the Raytheon Tin Whisker Core Team, and is the engineering lead for the Raytheon REACH



implementation project. David developed the Raytheon policy for tin whisker mitigation, and the IDS standard practices for tin whisker mitigation. David is a member of the Lead-Free in Aerospace Project – Working Group (LEAP-WG) tin whisker subcommittee. He has made multiple publications and presentations in the areas of tin whisker risk management, tin whisker risk assessments, and tin whisker growth mechanisms. He authored a chapter on reliability in a book entitled *Green Electronics*, which was published in 2008. David developed, published, and maintains a tin whisker risk assessment tool that is used widely across aerospace industry.

### **Anthony J. Rafanelli**

Dr. Anthony J. Rafanelli has thirty (30) years of service with the Raytheon Company. In his present role, he is an Engineering Fellow in the Mechanical Engineering Directorate currently assigned as the Hardware Lead Engineer for the Mission Systems Equipment (MSE) segment of the U.S. Navy Zumwalt destroyer program. He also serves on the Raytheon corporate RoHS team primarily focused on assessing impact, risk, and subsequent mitigation strategies regarding lead-free technology. This activity also includes active participation in the AIA PERM-LEAP Working Group as team lead for GEIA-STD-0005-3 document team and a participating member of the GEIA-HB-0005-1 and GEIA-HB-0005-2 document teams. He is also a Raytheon representative to the DoD ELF IPT. Experience includes materials science/engineering, mechanical engineering, components engineering, failure analysis, process development, process monitoring, quality control, reliability, quality management, systems engineering, engineering process, and engineering management.

He has earned the B.S. (1978), M.S. (1985) and Ph.D. (1995) degrees in Mechanical Engineering and Applied Mechanics from the University of Rhode Island. He is a licensed professional engineer in the states of Rhode Island and Massachusetts. He was a recipient of the Raytheon Excellence in Technology Award (2000).

He has published over sixty (60) papers, articles, and reviews in mechanical engineering, materials science/engineering (including lead-free technology), failure analysis, engineering management and general engineering. He is a member of the American Society of Mechanical Engineers (ASME), ASM International, and the Navy League of the United States, National Defense Industrial Association, and the Surface Mount Technology Association. In addition, he is a member and past-chair of the Industry Advisory Board (IAB) of the University of Maryland Computer-Aided Life Cycle Engineering Electronic Products and Systems Consortium. He is also serves on the Industry Advisory Councils of the University of Rhode Island College of Engineering, Mechanical Engineering, and Ocean Engineering Departments.

### Richard R. Reilly

Richard R. Reilly holds the Ph.D. in Organizational Psychology from the University of Tennessee and is Emeritus Professor in the Howe School of Technology Management. Before joining Stevens, Dr. Reilly was a research psychologist for Bell Laboratories, the Educational Testing Service and AT&T. He has been a consultant to Fortune 500 and governmental organizations on issues related to organizational performance. He is on the Editorial Board of Personnel Psychology and the International Journal of e-Collaboration and is a Fellow of the American Psychological Association and the American Psychological Society. He has co-authored four books including, *Blockbusters: Developing Award Winning New Products* (2002), *The Human Side of Project Leadership* (2007) and *Uniting the Virtual Workforce* (2008) and over 70 publications related to organizational behavior and project and team performance. His current research interests center on aspects of virtual work including leadership and trust.

### Polina Snugovsky

Polina Snugovsky (Ph.D.) is a Chief Metallurgist at Celestica. She is currently focused on lead-free and mixed lead-containing solder/lead-free component assembly, failure analysis, and whisker formation. Since 1999, she originated and facilitated four lead-free assembly and rework development projects that included extensive reliability testing at Celestica. She has actively participated in the iNEMI consortia for lead-free assembly and rework, with emphasis on failure analysis, and worked closely with other industry leading researchers. Since 2005, she has worked with the Lead-free Electronics in Aerospace Project Working Group (AIA LEAP WG). She supported the lead-free technical guidelines document GEIA-HB-0005-2, the Rework and Repair Handbook GEIA-STD-HB-0005-3, and the lead-free solder test protocol document GEIA-STD-0005-3. She is participating in the NASA-DoD lead-free reliability test project. Polina is a key figure in the understanding and mitigation of black pad failures on ENIG PCBs, in development of a plasma cleaning process and related laboratory methods for contamination (failure) analysis, and in major soldering-related failure analysis. Dr. Snugovsky graduated from the State Metallurgical Academy of Ukraine and received her Ph.D. in Metallurgy, and subsequently in 1985 she earned the higher level Doctoral degree in Metallurgy and Material Science. Before she joined Celestica in 1996, she was a full professor in the department of physical metallurgy of the State Metallurgical Academy of Ukraine. She is a specialist in eutectic materials and has more than 25 years of experience in solidification, phase transformation, microstructure interpretation, and metallographic techniques. She has published over 140 papers and patented new materials and processes. She holds several Outstanding Technical Achievement Awards, including two from Celestica.

**Fred W. Verdi**

Fred W. Verdi, is a Senior Manufacturing Engineer at ACI Technologies, Inc. He received his Master of Science degree in Metallurgy/Materials Science from Carnegie Mellon University, Pittsburgh, Pennsylvania and his BSME at the New Jersey Institute of Technology at Newark, New Jersey. Mr. Verdi has over 31 years of experience from Lucent Technologies and AT&T. This includes extensive managerial and design experience in a wide range of high technology electronics disciplines, including printed wiring board fabrication, supply chain analysis, risk mitigation for components, and new product development for Third Generation Wireless Base Station Products. He is an expert in electronics packaging technology including PWBs, HDI, BGA, and CSP, RF design, and layout for EMC and product miniaturization. Mr. Verdi has been with ACI Technologies for eight years, and is currently managing technical aspects of manufacturing in Miniaturized Military Electronics, COTS Electronics, Electrical Power components, and Lead-Free Electronics.

**Paul T. Vianco**

Paul T. Vianco received a Ph.D. degree in Materials Science from the University of Rochester (New York) in 1986. He joined Sandia National Laboratories, Albuquerque, New Mexico in 1987 where he is currently a distinguished member of the technical staff. Paul has been involved in all aspects of packaging interconnection technology: materials, processing, and reliability. In particular, his team has developed a methodology for qualifying the reliability of solder interconnections in complex satellite electronics using a combination of computational modeling and validation testing. Paul is a fellow of the American Welding Society (AWS) and currently chairman of the AWS C3 Brazing and Soldering Committee. Paul is the author of the *Soldering Handbook – Third Edition*, which is published by the AWS.

**Maureen Williams**

Maureen Williams is a Mechanical Engineer in the Metallurgy Division of the Materials Science and Engineering Laboratory (MSEL) at the National Institute of Standards and Technology (NIST) in Gaithersburg, Maryland. Her career at NIST started in 1988 as an undergraduate student. She graduated from the University of Maryland with a bachelor's degree in mechanical engineering in 1991 and a master's degree in materials science in 1999. Her research is focused on Sn whiskers. Since 1999 she has been involved in the International Electronics Manufacturing Initiative (iNEMI) Sn whisker projects and from 2001 until 2007 was co-chair of the iNEMI Sn Whisker Modeling Group. She is currently the project leader of the NIST Sn Whisker Project. This project is working on the fundamental growth mechanism of Sn whiskers. Her areas of interest include scanning electron microscopy (SEM), focused ion beam (FIB), and x-ray diffraction.

### **Thomas A. Woodrow**

Dr. Woodrow has worked for 26 years in the aerospace industry. Since 1997 he has been employed by Boeing and works in the Electronic Materials Technology Group which does R&D on electronics packaging. Dr. Woodrow is an experienced reliability engineer and conducted the thermal cycle, thermal shock and vibration testing for the Joint Council on Aging Aircraft/Joint Group on Pollution Prevention (JG-PP) Lead-Free Solder Project. He is also performing the thermal cycle, vibration and mechanical shock testing for the current NASA/DoD Lead-Free Electronics Project. Dr. Woodrow has used the JG-PP test data to validate various thermal cycle and vibration life prediction models. Dr. Woodrow is a founding member of the Tin Whisker Alert Group and is actively involved with the iNEMI Tin Whisker Test Methods Group which is exploring the basic mechanisms behind tin whisker growth. Dr. Woodrow has extensive experience with the use of conformal coatings for mitigating tin whisker growth. He has also conducted diffusion experiments to measure the grain boundary and lattice diffusion rates of tin within tin plated layers and has used isotopic Sn tracers to follow the diffusion of tin throughout a tin plated layer and into whiskers that grew on the plated layer.

### **Linda Woody**

Linda Woody is a process engineering manager for Lockheed Martin Missiles and Fire Control Systems. Linda has over 30 years of experience in Electronic and Electro Optical Design and assembly. As the Engineering Manager of the Production Development Center and the Advanced Services Laboratory, Linda has enacted various programs in Lockheed Martin; responsibilities include the development and improvement of various electronic manufacturing processes, prototype assembly, as well as concurrent engineering reviews of new design technologies. She continues to be an active member and leader of multiple internal corporate and industry committees including Corporate Lead-free working group, BGA working group, CCA complex commodity working group, various IPC committees, LEAP (Lead-Free Electronics Aerospace Project), and ELF (Executive Lead Free) working group. She has published articles in multiple magazines, and presented papers at numerous conferences including Nepcon, APEX, and DMC 2001-2007. She also holds a patent for laser soldering process technology.

# References

## CHAPTER 3

- [1] Becker J.H. "On the Quality of Gray Tin Crystals and Their Rate of Growth," Journal of Applied Physics Vol. 29 No. 7, July 1958.
- [2] Borgesen, P. "Lead-Free Solder Joint Reliability," Presentation at the 20th AIA Lead-free Electronics in Aerospace Project Working Group (LEAP-WG), Ft. Worth, Texas, January 27-29, 2009.
- [3] Dasgupta, Abhijit. "Pb-free Solder Interconnect Reliability Gaps," University of Maryland, Center for Advanced Life Cycle Engineering, Workshop on Testing Lead-free Electronic Assemblies, April 14, 2009.
- [4] GEIA-STD-0005-1, "Performance Standard for Aerospace and High Performance Electronic Systems Containing Pb-free Solder."
- [5] GEIA-STD-0005-2, "Standard for Mitigating the Effects of Tin Whiskers in Aerospace and High Performance Electronic Systems."
- [6] GEIA-HB-0005-1, "Program Management/Systems Engineering Guidelines for Managing the Transition to Pb-free Electronics."
- [7] GEIA-HB-0005-2, "Technical Guidelines for Aerospace and High Performance Electronic Systems Containing Pb-free Solder and Finishes."
- [8] GEIA-STD-0005-3, "Performance Testing for Aerospace and High Performance Electronic Interconnects Containing Pb-free Solder and Finishes."
- [9] GEIA-HB-0005-3, "Guidelines for Repair and Rework of Pb-free Assemblies Used in Aerospace and High-Performance Electronic Applications" (provisional title).
- [10] European Union, February 13, 2003. Directive 2002/95/EC/ of the European Parliament and of the Council of 27 January 2003 on the restriction of the use of certain hazardous substances in electrical and electronic equipment. Official Journal of the European Union.
- [11] B. Sorensen. "Digital Averaging – The Smoking Gun Behind 'No Fault Found'" Air Safety Week, February 24, 2003.
- [12] Sandborn, P. Lead-free Use Dynamic Simulator, CALCE University of Maryland.
- [13] P. Borgesen, E. Cotts, L. Yin, P. A. Kondos, B. Roggeman, P. Tumne, J. Li, and K. Srihari. "Interconnect Reliability in Medical Microelectronics Applications," Proc. SMTA Med. Electr. Symp., Anaheim, 2008.

## References

---

- [14] "Recommendations on Lead-Free Finishes for Piece-Parts Used in High Reliability Products," iNEMI Tin Whisker User Group, Herndon, VA USA, Version 4, Updated December 2006.  
[http://thor.inemi.org/webdownload/projects/ese/tin\\_whiskers/Pb-Free\\_Finishes\\_v4.pdf](http://thor.inemi.org/webdownload/projects/ese/tin_whiskers/Pb-Free_Finishes_v4.pdf)  
and J. Smetana, iNEMI Updates Tin Whisker Recommendations, Global SMT & Packaging, June 2007.
- [15] Galyon, G.T. and Ron Gedney R. "Avoiding Tin Whisker Reliability Problems," *Circuits Assembly*, August 2004.
- [16] Davy, G. "Relay Failure Caused by Tin Whiskers," Northrop Grumman Electronic Systems, Baltimore, MD, 2002.
- [17] Barry, N. "Soldering and Surface Mount Technology," V19 No2, 2007.
- [18] GEIA-HB-0005-4, "Guidelines for Performing Reliability Predictions for Pb-free Assemblies Used in Aerospace and High-Performance Electronic Applications" (in work).
- [19] Liu, W. and Lee, N-C. "The Effects of Additives to SnAgCu Alloys on Microstructure and Drop Impact Reliability of Solder Joints," JOM Vol. 59, No.7, July, 2007, pp. 26-31.
- [20] Meschter, S. "Tin Whisker Risk," IEEE ASTR (Accelerated Stress Testing and Reliability) Conference, Portland, Oregon, October 1-3, 2008.
- [21] CALCE Research on Risk Assessment, Management, and Mitigation Research for Pb-free Electronics at CALCE presented at the ACI Lead Free Summit held on July 13, 2005 in Philadelphia, PA, <http://www.calce.umd.edu/tin-whiskers/publications.html>.
- [22] Pinsky, D. "An Updated Application-Specific Tin Whisker Risk Assessment Algorithm Within A Process Compliant to GEIA-STD-0005-2," Raytheon Company, March 2007.

## Other Chapter 3 References

- [Smetana 2009] Smetana, J., Sack, T., Rothschild, W., Birch, B., and Morton, K. "Bare Board Material Performance after Pb-free Reflow," IPC/APEX March 31 - April 2, 2009.
- [Woodrow 2006] Woodrow, T.A. and Ledbury, E.A. "Evaluation of Conformal Coatings as a Tin Whisker Mitigation Strategy, Part II," SMTA International Conference Proceedings, 2006.
- [Winkler 2008] Winkler, J. et.al. "Tin Whisker Containment with Flexible Ceramic Conformal Coatings," Defense Manufacturing Conference 2008, December 3, 2008.
- [Sanborn 2] Sandborn, P. Part Total Ownership Model. CALCE University of Maryland.
- [Schueller 2007] Schueller, R. "Creep Corrosion of Lead-Free PCBs," SMTA International 2007.

- [Kadesch 2000] Kadesch, J. and Leidecker, H. "Effects of Conformal Coat on Tin Whisker Growth," IMAPS Nordic Conference 2000
- [Lall 2009] Lall, P. "An Overview of Research Activities in Lead-Free Solders, NSF Center for Advanced Vehicle and Extreme Environment Electronics," presented at the AIA-PERM (Aerospace Industries Association Pb-free Risk Management) Consortium meeting, Huntsville, Maryland, May 19-21, 2009.
- [Courey 2009] Karim J. Courey, K. et.al. "Tin Whisker Electrical Short Circuit Characteristics - Part II," IEEE Trans on Electronics Packaging Manufacturing, V32, No. 1, January 2009.

## CHAPTER 4

- [1] IPC 6012
- [2] IPC J-STD 003
- [3] IPC 1601
- [4] IPC J-STD-075
- [5] IPC J-STD-020
- [6] IPC J-STD-033
- [7] GEIA-STD-0005-1
- [8] J-STD-020(C)
- [9] P. Snugovsky, et al. "Microstructure, Defects, and Reliability of Mixed Pb Free/SnPb Assemblies," Proceedings TMS, V1: Materials Processing and Properties, p.p. 631-642, 2008.
- [10] "Real Life Tin-Silver-Copper Alloy Processing," A. Rae et al. APEX Conference Proceedings.
- [11] R. Kinyanjui, Q. Chu, P. Snugovsky and R. Coyle. "Solder Joint Reliability of Pb-free Sn-Ag-Cu Ball Grid Array (BGA) Components in Sn-Pb Assembly Process," proceedings APEX, 2008.
- [12] "Effect of SnAgCu Composition on Reflow Behavior," Dr. B. Huang, Dr. A. Dasgupta and Dr. N-C Lee, Indium Corporation of America, Amsterdam, 2004.
- [13] C. Hamilton, P. Snugovsky, Celestica Inc. and M. Kelly, IBM Corporation, "Have High Cu Dissolution Rates of SAC305/405 Alloys Forced a Change in the Pb-free Alloy Used during PTH Processes?" Pan Pacific Microelectronics SMTA Conference, 2007.

## References

---

- [14] C. Hamilton, Celestica Inc. and M. Kelly, IBM Corporation. "A Study of Alternative Pb-free Wave Alloys: Form Process Yield to Reliability," APEX Conference, 2008.
- [15] U.S. Environmental Protection Agency, "Solders in Electronics: A Life Cycle Assessment," EPA Report 744-R-05-001, February 2005, EPA *Design for the Environment* program.
- [16] "Pb-free Technology and the Necessary Changes in Soldering Process and Machine Technology," H. Schlessmann, APEX 2002 Conference Proceedings.
- [17] U.S. Environmental Protection Agency, "Solders in Electronics: A Life Cycle Assessment," EPA Report 744-R-05-001, February 2005, EPA *Design for the Environment* program.
- [18] IPC-A-610
- [19] IPC-CC-830B
- [20] GEIA STD-0005-2

### Other Chapter 4 References

"Dissolution rates of iron plating on soldering iron tips in molten Pb-free solders," Takemoto et al. *Soldering & Surface Mount Technology*, Vol. 16, No. 3, 2004.

"Under The Plating," American Hakko Products Technical Report, July 2002.

P. Snugovsky, Z. Bagheri, M. Kelly, M. Romansky. "Solder Joint Formation with Sn-Ag-Cu and Sn-Pb Balls and Pastes," SMTA International Conference Proceedings, September 2002, pp. 823-834.

M. Kelly, M. Ferrill, P. Snugovsky, Rupen Trivedi, Gaby Dinca, Chris Achong, Zohreh Bagheri. "Rework Process Window and Microstructural Analysis for Pb-free Mirrored BGA Design Points," Conference Proceedings, APEX 2009.

K. Seelig and D. Suraski. "Lead Contamination in Pb-free Electronics Assembly," <http://www.aimsolder.com/techarticles/Lead%20Contamination%20in%20Pb-free%20Electronics%20Assembly.pdf>.

G. Henshall. "iNEMI Alternatives Project Report: State of the Industry," Proceedings, SMTA International, 2008.

B. Smith, P. Snugovsky, M. Brizoux and A. Grivon. "Industrial Backward Solution for Pb-free Exempted AHP Electronic Products: Process Technology Fundamentals and Failure Analysis," Proceedings IPC APEX, April 2008.



M. Kelly, et al. "Pb-Free Assembly and Rework" (iNEMI project), Proceedings APEX, 2005.

"Reliability and Failure Mechanisms of Laminate Substrates in a Pb-free World," Kevin Knadle, Endicott Interconnect Technologies, Inc., Endicott, NY.

## CHAPTER 5

[1] GEIA-STD-0005-1, "Performance Standard for Aerospace and High Performance Electronic Systems Containing Lead-free Solder," 15 June 2006.

[2] MIL-STD-3018, Parts Management.

[3] ANSI/EIA-649, "National Consensus Standard for Configuration Management," 28 October 2004.

[4] IPC/JEDEC J-STD-609, "Marking and Labeling of Components, PCBs and PCBA's to Identify Lead (Pb), Pb-Free and Other Attributes," 1 May 2007.

[5] EIA-933, "Standard for Preparing a COTS Assembly Management Plan," December 2002.

[6] IEC TS 62239, "Process Management for Avionics - Preparation of an Electronic Components Management Plan - Edition 2.0," 1 October 2008.

[7] MIL-HDBK-502, Acquisition Logistics, 30 May 1997.

[8] IPC J-STD-001D, "Requirements for Soldered Electrical and Electronic Assemblies," 1 February 2005.

[9] IPC-7711/7721B, "Rework, Modification and Repair of Electronic Assemblies," November 2007.

[10] GEIA-STD-0005-2, "Standard for Mitigating the Effects of Tin Whiskers in Aerospace and High Performance Electronic Systems," 1 June 2006.

[11] GEIA-HB-0005-3, "Rework/Repair Handbook to Address the Implications of Lead-Free Electronics and Mixed Assemblies in Aerospace and High Performance Electronic Systems," 1 September 2008.

[12] ARINC 671, "Guidance for the Transition to Lead-Free Soldering, Maintenance, and Repair," 15 March 2006.

### CHAPTER 6

- [1] K. N. Tu, M. Y. Yan, Fei Ren, Joanne Huang, Emily Ou, L. Y. Zhang, and J. W. Nah. "Electromigration in Flip Chip Solder Joints," AIP Proceedings of 8th Workshop on Stress-Induced Phenomena in Metallization, Dresden, Germany, vol. 817, p. 327-338, 2006.
- [2] Jae-Woong Nah, Fei Ren, Kyung-Wook Paik, and K. N. Tu. "Effect of Electromigration on Mechanical Shear Behavior of Flip Chip Solder Joints," J. Mater. Res., 21, 698-702, 2006.

### CHAPTER 7

- [1] Bieler, T. R., Jiang, H., Lehman, L. P., Kirkpatrick, T. and Cotts, E.J. "Influence of Sn Grain Size and Orientation on the Thermomechanical Response and Reliability of Pb-free Solder Joints," Proc. ECTC 2006, pp. 1467-7.
- [2] B. Arfaei, Y. Xing, J. Woods, J. Wolcott, P. Tumne, P. Borgesen and E. Cotts. "The Effect of Sn Grain Number and Orientation on the Shear Fatigue Life of SnAgCu Solder Joints," Proc. ECTC 2008, 459-465.
- [3] P. Borgesen, E. Cotts, L. Yin, P. A. Kondos, B. Roggeman, P. Tumne, J. Li and K. Srihari. "Interconnect Reliability in Medical Microelectronics Applications," Proc. SMTA Med. Electr. Symp., Anaheim 2008.
- [4] Dasgupta, A. "Pb-free Solder Interconnect Reliability Gaps," Pb-free Electronics Manhattan Project Briefing, April 20, 2009.
- [5] "Guidelines for Accelerated Reliability Testing of Surface Mount Solder Attachments," IPC-SM-785, November 1992.
- [6] "Design Guidelines for Reliable Surface Mount Technology Printed Circuit Boards," IPC-D-279, July 1996.
- [7] "Guidelines for Performance Test Methods and Qualification Requirements for Surface Mount Solder Attachments," IPC-9701, January 2002.
- [8] Norris, K. C. and A. H. Landzberg, A. H. "Reliability of Controlled Collapse Interconnections," *IBM Journal of Research and Development*, May 1969, pp. 266-271.
- [9] W. Engelmaier. "Fatigue Life of Leadless Chip Carrier Solder Joints During Power Cycling," *IEEE Transactions on Components, Hybrids and Manufacturing Technology*, Vol. CHMT-6, No. 3, pp. 232-237, 1983.

- [10] A. Dasgupta, C. Oman, D. Barker and M. Petit. "Solder Creep-Fatigue Analysis by an Energy-Partitioning Approach," *ASME Journal of Electronic Packaging*, Vol. 114, No.2, pp.152-60, 1992.
- [11] Clech, J-P. "Solder Reliability Solutions: a PC-Based Design-for-Reliability Tool," Proceedings, Surface Mount International Conference, Sept.-12, 1996, San Jose, CA, pp. 136-151.
- [12] A. Syed. "Accumulated Creep Strain and Energy Density Based Thermal Fatigue Life Prediction Models for SnAgCu Solder Joints," Proceedings of Electronic Components and Technology Conference, Vol. 1, pp. 94-99, 2004.
- [13] O. Almelo, K. Anderson, A. Portola, J. Parka and M. Tasmania. "Re-calibration of Engel Maier's Model for Leadless, Pb-free Solder Attachments," *Quality and Reliability Engineering International*, Vol. 23, pp. 415-429, 2006.
- [14] M. Osterman and M. Petit. "Strain Range Fatigue Life Assessment of Pb-free Solder Interconnects Subject to Temperature Cycle Loading," *Soldering & Surface Mount Technology*, Vol. 19, No. 2, pp. 12-17, 2007.
- [15] W. Engelmaier. "Creep-Fatigue Model for SAC405/305 Solder Joint Reliability Estimation - A Proposal," *Global SMT and Packaging*, Vol. 8, No. 12, 2008.
- [16] Schubert, A., Dudek, R., Auerswald, E., Gollhardt, A., Michel, B. and Reichl, H. "Fatigue Life Models for SnAgCu and SnPb Solder Joints Evaluated by Experiments and Simulation," 53rd ECTC, 2003, pp. 603-610.
- [17] V. Vasudevan and X. Fan. "An Acceleration Model for Pb-free (SAC) Solder Joint Reliability under Thermal Cycling," 2008 Electronic Components and Technology Conference, pp 139-145.
- [18] N. Pan, G. Henshall, R. Lewis, E. Benedetti and J. Rayners. "An Acceleration Model for Sn-Ag-Cu Solder Joint Reliability under Various Thermal Cycle Conditions," Proc. SMTA, 2005, pp. 876-883
- [19] Ron Zhang, Jean-Paul Clech. "Applicability of Various Pb-free Solder Joint Acceleration Factor Models," SMTA International, 2006.
- [20] W. Dauksher. "A Second Level SAC Solder-Joint Fatigue Life Prediction Methodology," IEEE Trans. Dev. Mater. Reliab. Vol. 8, No. 1, pp. 168-173, 2008.
- [21] S.S. Manson. "Thermal Stress and Low Cycle Fatigue," McGraw-Hill, New York, 1966.

## References

---

- [22] J.D. Morrow. "Cyclic Plastic Strain Energy and Fatigue of Metals," ASTM STP 378, Philadelphia, pp. 45-87, 1964.
- [23] A. Choubey, M. Osterman, M. Pecht and D. Hillman. "Durability of Repaired and Aged Pb-free Electronic Assemblies," IPC Printed Circuits Expo, APEX, and Designers Summit, Los Angeles, CA. Feb 18-22, 2007.
- [24] John Manock, Richard Coyle, Brian Vaccaro, Heather McCormick, Richard Popowich, Debra Fleming, Peter Read, John Osenbach and Dan Gerlach. "Effect of Temperature Cycling Parameters on the Solder Joint Reliability of A Pb-Free PBGA Package," SMTAI, 2006, pp. 564-574
- [25] Y. Zhou and A. Dasgupta. "Vibration Durability Assessment of Sn3.0Ag0.5Cu & Sn37Pb Solders under Harmonic Excitation," 2007 ASME International Mechanical Engineering Congress and Exposition, Seattle, Washington, November 11-17, 2007.
- [26] Steinberg. "Vibration Analysis for Electronic Equipment," Wiley, 2000.
- [27] JEDEC JESD22-B111, "Board Level Drop Test Method of Components for Handheld Electronic Products."
- [28] JEDEC 104C
- [29] JEDEC 110A
- [30] JEDEC 111B
- [31] MIL-STD-810, Method 516.5
- [32] P. Borgesen and E. Cottis. "Implantable Medical Electronics Assembly - Quality and Reliability Considerations," Proc. SMTA Medical Symp., Minneapolis, MN, 2004.
- [33] Donald Cullen, Witold Paw, John Swanson and Lenora Toscano. "Eliminating Microvoid Risk Via. An Optimized Surface Finish Process," <http://www.pcb007.com/pdf/Cullen-CMAP-Manuscript.pdf>.
- [34] L. Yin et al. "Controlling Cu Electroplating to Prevent Sporadic Voiding in Cu3Sn," Proc. ECTC 2009.
- [35] K. Upadhyayula and A. Dasgupta. "An Incremental Damage Superposition Approach for Interconnect Reliability Under Combined Accelerated Stresses," ASME International Mechanical Engineering Congress & Exposition, Dallas, TX, November 16-21, 1997.

- [36] H. Qi, M. Osterman and M. Pecht. "Design of Experiments for Board Level Solder Joint Reliability of PBGA Package under Various Manufacturing and Multiple Environmental Loading Conditions," IEEE Transactions on Electronics Packaging Manufacturing, 2007.
- [37] Pecht and Ganesan. "Pb-free Electronics," Wiley, 2006.
- [38] Limaye, P., Maurissen, W., Lambrinou, K., Duflos, F., Vandeveld, B., Allaert, B., Hillaert, J. and Vandepitte, B. "Low-Temperature Embrittlement of Pb-free Solders in Joint Level Impact Testing," 9th EPTC, pp. 141-151, 2007.
- [39] Suhling, J. "Material Behavior of Aging Pb-free Solder Joints," Pb-free Electronics Manhattan Project Briefing, April 21, 2009.
- [40] CALCE
- [41] Rockwell Collins
- [42] R. C. Lasky. "Tin Pest: A Forgotten Issue in Pb-free Soldering?"  
<http://www.indium.com/drlasky/files/TinPestPaper0723Final.pdf>.
- [43] D. Yoder, S. Bhandarkar and A. Dasgupta. "Experimental and Analytical Investigation of PTH Fatigue Life in Aramid PCBs - Part II," IPC Review, June 1993 (part 2).
- [44] B. Rudra, M. Pecht and D. Jennings. "Assessing Time-to-Failure Due to Conductive Filament Formation in Multi-Layer Organic Laminates," IEEE Transactions on Components, Packaging and Manufacturing Techniques - Part B, Vol. 17, No. 3, pp. 269-276, August 1994.
- [45] B. Rudra and D. Jennings. "Tutorial," IEEE Transactions on Reliability, Vol. 43, No. 3, September, 1994.
- [46] Smetana, J. "Bare Board Material Performance after Pb-free Reflow," Pb-free Electronics Manhattan Project Presentation, April 20, 2009.
- [47] Schueller, R. "Major Issues Encountered with LF Transition," Pb-free Electronics Manhattan Project Presentation, April 26, 2009.
- [48] <http://nepp.nasa.gov/whisker/failures/index.htm>

## References

---

- [49] T. Fang, M. Osterman and M. Pecht. "Statistical Analysis of Tin Whisker Growth," *Microelectronics Reliability*, Vol. 46, Issues 5-6, pp. 846-849, May-June, 2006.
- [50] JESD-201
- [51] "A Tin Whisker Risk Assessment Algorithm,"  
<https://www.reliabilityanalysislab.com/TechnicalLibraryTinWhisker.asp>.
- [52] Tong Fang, Michael Osterman and Michael Pecht. "Reliability I (Issues in Packaging)," 38th International Symposium on Microelectronics, pp. 61-65, Philadelphia, PA, September 25-29, 2005.
- [53] Final Report on the Transformational Manufacturing Technology Initiative (TMTI), ManTech Research Project S1057.
- [54] V. Venkatadri, L. Yin, Y. Xing, E. Cotts, K. Srihari and P. Borgesen. "Accelerating the Effects of Aging on the Reliability of Lead Free Solder Joints in a Quantitative Fashion," Proc. ECTC, 2009.
- [55] P. Borgesen, M. Meilunas and E. Al-Momani. "Effect of Dwell Time on the Life of Lead Free BGA Joints in Thermal Cycling," to be published in Proc. SMTA Int. 2009.
- [56] M. Osterman
- [57] Cuddalorepatta, G. and Dasgupta, A. "Optimization of Dwell Time for Accelerated Thermal Cycling of Sn3.0Ag0.5Cu Pb-Free Interconnects," July 2007, IISc Centenary - International Conference on Advances in Mechanical Engineering (IC-ICAME), Bangalore, India.
- [58] Syed, A. "Reliability and Au Embrittlement of Lead Free Solders for BGA Applications," Proceedings. International Symposium on Advanced Packaging Materials: Processes, Properties and Interfaces, 11-14 March 2001, pp. 143 - 147.
- [59] Jin Yu and J.Y. Kim. "Effects of Residual S on Kirkendall Void Formation at Cu/Sn-3.5Ag Solder Joints," *Acta Materialia*, pp. 5514-5523, 2008.

# Index

## A

- accelerated life testing (ALT) 49, 97-8, 101, 210, 271
- Accelerated Reliability Testing 269
- Accelerated Reliability Testing Validation 207
- Accelerated Temperature and Humidity Stress Test 210, 271
- acceleration factor (AF) 52-3, 98-9, 102, 194, 221-3, 225, 232, 279-80, 282
- acceptance 19, 77, 99, 101-2, 182-3, 185, 190, 192-4, 204-8, 260, 273
- acceptance criteria 71-2, 79, 189
- A&D 2, 27, 30, 33-4, 103, 108, 173, 206, 239
- A&D applications 30, 53, 56, 62, 85-6, 88, 167, 174, 177, 183, 189-90, 230, 246, 248, 252-3
- A&D assemblies 58, 174-5, 177-8
- A&D control 44-5
- A&D designs 14
- A&D electronics 185, 190, 192-4
- A&D equipment 14, 43, 95-6, 106, 108
- A&D industry 54, 59-60, 62, 66, 70-2, 74, 77, 81-2, 104, 172-3, 177, 238
- A&D OEMs 2, 6-7, 44
- A&D products 7, 22-3, 30, 49-50, 56, 90, 183, 219, 224, 227, 230, 238, 246-7
- A&D programs 41, 44, 67, 168, 173, 182, 213, 240, 243, 246
- A&D repair facilities 173, 176, 179
- A&D systems 109, 182, 214, 238-40
- A&D users 44-5
- Adequate for Pb-Free 185, 204, 206, 209
- aerospace 2, 9, 12, 22-3, 52, 60, 190, 256, 261, 281
- Aerospace Industries Association see AIA
- AF see acceleration factor
- Ag3Sn 130-4
- aging 92-3, 209, 223, 226, 231-2, 236, 280
- AIA (Aerospace Industries Association) 9-11, 52, 167, 256
- air rework, hot 158
- airborne equipment 52
- alloys 19-20, 36, 47, 50, 56, 68-70, 72, 74, 76-7, 125-6, 141, 159, 165, 176, 274, 278
- eutectic 19, 124, 282
- low Ag 137, 140, 143
- mixed 222-3, 225-6
- new 32, 56-7, 94
- ALT see accelerated life testing
- AMRDEC 10-11, 285
- Annealing Treatments 195, 262, 274
- Applicable Standard 185-92, 195-201, 203-11, 258-61, 266, 268-72
- applications 20, 44, 48, 54, 62, 73-4, 78, 97, 106, 111, 128, 154-5, 229, 231-2, 261, 279-80
- approach, baseline practice qualification test 50, 53
- article inspections, first 116, 121, 244, 251
- artifacts iii, 288
- assemblies 1, 30-2, 44-5, 74, 81-3, 88-9, 112, 121-2, 135-6, 140, 172-3, 175-7, 229, 232-4, 243-5, 252-3
- electrical 27, 82
- lead-free 306
- original 144, 165, 178-9, 245
- printed wiring 121
- soldered 15, 27, 41, 72, 83, 87-8, 95, 233
- assembly alloys 167, 177, 179
- assembly solder 16-18, 26, 168, 171
- common Pb-free 77
- assembly solder alloys 28, 173, 178
- assessment 22, 32, 52, 71, 96-7, 112, 152, 162-3, 166, 187, 261-2

ASTM test methods 196, 199-200, 202  
    relevant 275-7

availability loss 247

awareness 6-7, 9, 78, 111

## B

baseline iii, 2-3, 243, 281, 288

Baseline Practice 16-18, 28, 185-92, 195-201,  
203-11, 229, 258-61, 266, 268-72, 288

Baseline Practice Test and Applicable Standard  
262-5, 267

Benchmarking and Best Practices Center  
of Excellence ii-iii

best practices ii-iii, 3, 32, 83-4, 111, 119, 215,  
217-18, 243, 254, 281, 283-5, 288, 292-6

Best Practices Summary 293-6

BGA components 73, 155

BGA reballing 58, 62, 66

Binghamton University see BU

board fabricators 116, 235, 238

boards 37, 80, 115, 117, 122-3, 126, 134, 138,  
143, 193

boiling point chemistry 150, 152

BOM 28, 66-7, 71, 244, 250

brass 67-9

breakout rooms 285, 292-3

BU (Binghamton University) 278-80

## C

CAF failures 236-7

CALCE v, vii, 10, 26, 236, 239, 279

CCA designs 160, 243

CCA level test results 236

CCA solder joints 82, 156

CCA wave solder processes 149, 152

CCAs (circuit card assembly) ix, 18, 21, 27, 35, 39,  
44, 61, 66-7, 70-1, 73-4, 81-2, 99, 107, 119, 123-4,  
152-4, 173, 183, 190, 261

CCAs and Pb-free solder joints 117

Celestica 127, 132, 137, 149

checkpoints 100

circuit, open 26, 38-9, 84

circuit card assembly see CCAs

class 2, 30, 36, 38, 65, 72, 104, 169, 185, 190,  
215-16, 239

Clean Ability 121

co-leaders 284-7, 289-92

coatings 62, 67, 71-3, 83, 104, 160, 239

color designations 119

Combined Loading 220, 223, 225, 227

Common Pb-free Solder Manufacturing 76

Common Pb-free Solders for Assembly  
and Sustainment 77

communication 81-2, 245, 252, 286-7, 298

compatibility 19-20, 28, 35, 74, 101, 121, 147,  
153-4, 169-70, 180, 230

compatibility issues 43, 117, 172

completion 48, 50, 55

compliance 33, 46, 51, 65, 67, 76, 121, 165,  
202, 267-8

component alteration processes 118

component construction materials 274-5

Component Danger Area 127

component issues 116, 121

component materials 196, 198

component placement viii, 123-4

component solderability 57, 189

component staking 229

Component Testing for Pb-Free CCAs 189

component types 69, 86, 134



components 10-11, 32-3, 45-6, 58, 69-71, 117-18, 121-2, 126-8, 136, 142-3, 153, 183-5, 189-90, 192-3, 218, 260-1

Computational model of package-on-package  
Pb-free solder 273

computational models 11, 49, 54-5, 98-9, 101-3, 182, 194, 200-1, 204-7, 244-5, 273-6

conditions 20, 35, 40-1, 48, 50, 52, 55, 104, 140, 217, 220-1, 230, 250-1  
default Pb-free test 206

configuration management ix, 8, 42-3, 57, 59-60, 166-7, 169, 245

conformal coating ix, 21, 24, 30, 59, 66-7, 71, 105, 115, 121, 154, 160-1, 239

constituents 18-19, 169

constitutive equation 195, 199, 274-6

content 105, 111, 169, 287, 289

contract 22, 40-1, 54, 102-3, 165

control 1, 43, 46, 59, 69, 80, 150, 152, 165, 167, 177, 216, 219, 232, 243, 248  
solder bath 144, 147, 149

control tin risk 31

controlled cooling rate requirement 146, 149, 152

coordinates 31, 179-80, 256

copper 75, 78, 87, 105, 124, 183-4, 188, 227, 235, 260

copper dissolution 19-21, 24, 125, 140, 144, 183, 193-4, 226, 235

Copper Foils 184, 188, 260

Copper Testing 188

corner 105, 220, 229-30

correlates 49, 53, 98-9, 101-2

corrosion 14, 19, 67, 79, 94, 104, 106, 108, 183, 192, 218, 237-8

corrosion failures 237-8

cost ii, iv, 8-11, 27, 47, 56-60, 100, 122, 124, 153, 167, 194, 239-40, 243, 248, 272  
energy 145-8

cost impact 57, 59-60

COTS 2, 8, 10, 30-1, 46, 84, 168, 170, 245, 252

COTS assemblies 168, 170

COTS components 57-8

coupons, designed test 236

cracking 117, 160, 162, 183, 224, 233, 235

cratering 226, 235-6

critical issues 10, 281

Cross-Compatibility of SnPb and Common  
Pb-free Solders 77

Cross contamination issues 123

Cu 68-9, 75, 124, 130, 134-5, 318

Cu dissolution 80, 140-2, 158

cultural issues 12

Current baseline practice for SnPb CCAs 193

current baseline practices iii, 12, 25, 166-7, 171, 173, 217, 248, 250, 253, 283

Current Test Equipment 185-92, 195-201, 203, 205, 207-8, 210-11

curve, bathtub 215-17

customer requirements 3, 18, 25, 28, 30, 32, 42-4, 167, 169-72, 174

customers 7, 22, 28, 30, 34-5, 45, 47, 49-50, 61-2, 66, 81-2, 84, 98-9, 109, 120, 166-7

cycles 51, 89-90, 95, 221, 224, 228, 278  
design-analysis-test 72

Cyclic Mechanical Properties 199, 202, 275, 278

cycling 228, 236, 278-9

## D

Dasgupta 222, 280

date Pb-free reliability knowledge 55

defects 76, 102, 135-6, 156-7, 162, 209, 217-19, 225-7, 236-7, 260, 271

degree 39, 45, 50, 114-15, 130, 140, 143, 158, 205, 229

- delamination 78-9, 118, 186-7, 218, 259
  - densities 70, 105-6, 217, 232
  - Department of Defense see DoD
  - design
    - electrical 70, 85
    - environmental 49
    - schematic 71, 85
  - design authorities 43, 172, 175, 177-9
  - design changes 49, 72, 87, 99, 102
  - design constraints 85-6
  - design documentation 21, 35
  - Design Element 27, 61-2
  - design engineers 192
  - design experience 229
  - design factors 105-6, 108
  - Design for Manufacturing see DFM
  - design guidelines 35, 94
    - heritage SnPb 86
  - Design in Product Development Cycle 15
  - design interface 43, 172
  - design life 74, 98
  - design limits 98-9
  - design optimization process 98-9
  - design parameters 82, 95
  - design phase 109, 239
  - design practices 28, 84
  - design process 18, 21, 47, 111
  - Design Reliability 214
  - design requirements 51, 97, 221
  - Design Review 36-7, 100
  - design review processes 84, 100
  - design rules 31, 56, 68, 83, 85, 94, 97, 116, 121, 153, 243, 251
    - heritage SnPb 72
  - Design rules of thumb for A&D
  - Pb-free products 86
  - design tests 182
  - Design Verification viii, 15, 27, 83, 102
  - Designed solder stress levels 21
  - designers 18, 23, 29, 45-6, 53, 66, 72, 75, 82, 90, 224, 229, 243-4, 252
  - devices 14, 69-70
  - DFM (Design for Manufacturing) viii, 42, 83, 115-16, 121, 163, 166, 244
  - diagnostic 172, 174
  - disparate Pb-free solders 229
  - Documentation 8, 112, 174, 176-8, 180
  - documents 2, 4, 7, 22, 28, 30, 51-3, 75, 101, 109-10, 171, 174, 176-7, 215, 239, 277-8
  - DoD (Department of Defense) 1, 9-10, 12, 33, 51, 173, 243, 256
  - DoD Soldering Technology Working Group 175, 178
  - Draft 186, 189, 258, 260
  - drafts 258, 260, 284, 288, 291
  - durations 47, 50, 52, 101, 279
- ## E
- early introduction of Pb-free interconnect technologies 39, 84
  - Effect of Alloy on Cu Dissolution Rates 141
  - effects of solder joint 272, 279
  - efforts i-ii, iv, 9-10, 12, 29, 85, 165, 169, 194, 205, 236, 243, 254, 256, 284
  - EIP (Electronic Information Product) 33
  - electromigration 70-1, 85-6, 185, 210, 217, 232-3, 258, 272
  - Electromigration Testing 185, 210
  - electronic assemblies 1, 14, 22, 32, 34, 97, 102, 120, 169, 183-4, 245-6, 248, 253
  - electronic equipment 6, 282
  - Electronic Information Product (EIP) 33
  - electronic parts 35, 61, 63, 250

electronic systems 22, 34, 59  
 design of 61, 251

electronics industry i, 32, 75, 146, 149, 154, 156, 246

electronics manufacturing, lead-free 281

Electronics Manufacturing Productivity Facility  
 see EMPF

Elevated Temperature 23, 188, 197, 240, 260, 263-4, 280

ELF IPT 9-11

elongation 188, 260

EMPF (Electronics Manufacturing Productivity Facility) 9-11

encapsulants 62, 71-3

enclosures 27, 61-2, 81-2

End-of-Life 146, 148, 216-18

Energy Dispersive Spectroscopy 122, 186, 189, 258, 260

Engelmaier 222, 279-80

Engelmaier Model 221, 279

engineering 39, 84, 98, 111

Engineering and Manufacturing R&D for Pb-Free Electronics Transition 60

ENIG boards 130

environmental conditions 26, 39, 46-7, 52, 109, 221, 244, 250, 253

Environmental stress screening see ESS

environments iii, 20, 25, 37, 47, 50, 52, 56, 63, 75-6, 86, 90, 106, 108, 209-10, 237-8

equipment 8-9, 34, 46, 51, 120-3, 144, 151-5, 158, 162, 173-5, 177-80, 182, 205-9, 211, 245

equipment configuration 145, 147

equipment parameters 123-4, 149, 154, 156-7

ESS (Environmental stress screening) 39, 50, 101, 115, 182, 205-8, 220, 227-8, 245-6, 250, 269-70

EU see European Union

European Union (EU) 1, 6, 34, 282

eutectic 14, 131, 134

Expansion of Solid Materials 200-1, 265-6

experience iii, 1, 20, 67, 75-7, 96, 176, 179, 230, 284, 288-9

experiments 279-80

expertise 243, 284, 289

experts 281-5

exposures, short-term solder 186, 259

extrapolation 7, 236, 279-80

## F

FAA (Federal Aviation Administration) 110, 256

facilities iv, 120, 174-5, 178

factors 1-2, 7, 16-18, 37, 54, 58, 70, 74, 114, 172, 177, 213, 226, 228, 236, 279

failure analysis 39, 201

failure mechanisms 40, 55, 101, 114, 116-17, 206, 215, 223, 269

Failure Mode Analysis 201, 203-4, 211

Failure Mode Analysis of Materials Test Specimens 201, 276

Failure Mode Analysis of Simulated Solder Joints 203, 278

failure models 103, 219, 231-2

failure modes 14, 17-18, 22, 37-8, 49, 52-6, 61, 70, 87, 98-100, 173, 193, 201, 216, 235, 244

failure point 207-8

failure rates 39, 68, 216

failure sources ix, 215, 217-19, 232

failures 8, 37-9, 45, 75-6, 82-3, 89-90, 92-3, 205-9, 215-18, 221, 224-8, 232-3, 235-6, 239-40, 245-6  
 complete 247  
 induced 109, 237-8  
 intermetallic 38, 55, 236  
 multiple 37-8

failures results 216

fatigue 25, 86, 95, 97, 217, 220

Fatigue life models 221

fault tree 36, 39, 73, 84-5

Federal Aviation Administration (FAA) 110, 256

feedback 98-9, 252, 286-7, 289, 291

FIB (focused ion beam) 201, 203, 210, 266, 268, 272

fidelity 204, 274-5

field conditions, expected 206-7, 269-70

field lifetimes 182, 206, 209, 211, 271

finish selection, component surface 124

finishes 8, 10, 20, 22-3, 52, 69-70, 82, 114, 122, 179-80, 182, 207, 240, 261, 269, 309-10

fluxes 24, 101, 120-1, 140, 153, 175-6, 178-80, 191, 261

FMEA 36-7, 39, 70-1, 73, 84, 244

FMECA 36-7, 70-1

focused ion beam see FIB

footprint 202, 267-8

formation 130, 182, 194

fracture surfaces 201, 203, 276, 278

## G

gaps iv, 2, 4, 12, 25, 44, 84-6, 110, 142-3, 166, 171, 177, 182, 227, 243, 267-8

GEIA-HB-0005 18, 22-3, 25, 28-9, 43, 48, 62, 66, 71, 75, 77, 84, 94, 108-10

GEIA-STD-0005 22, 27-32, 37, 43, 45, 52-6, 66-7, 81-2, 95-6, 100, 106, 167, 175-7

General Design Recommendations 250

General Pb-Free Solder Alloy Behavior 23

Generation of Pb-free design rules 103

## H

HALT (highly accelerated life testing) 49, 98, 101, 209-10, 227-8, 271

handling 16, 79-81, 106, 108, 123-4, 149, 154, 162-3, 174, 177, 180, 204, 227

handling procedures 173, 175, 177-9

hardware design viii, 15, 27, 35, 61-2, 98, 102

hardware design elements 61-2

hardware design processes 61

hardware designers 62, 66, 99

hardware loss 247

hardware over-design 194, 273

HASL (hot air solder leveled) 194

HAST (highly accelerated stress testing) 98-9, 209-10, 271

High Performance Electronic Interconnects  
Containing Pb-free 207, 269

High Performance Electronic Systems  
Containing Pb-free 23

High Risk 15, 17-18, 21, 27, 36, 48, 61, 75-6, 134

high temperature 78, 119, 209

highly accelerated life testing see HALT

highly accelerated stress testing see HAST

hot air solder leveled (HASL) 194

hot solder dipping 23, 118

humidity 14, 19, 46-7, 94, 106, 108-9, 190, 205, 209, 218, 230

Humidity Testing 205, 268

## I

IAB (Industrial Advisory Board) 9-10, 283-4

images 72, 91, 105, 118-19, 131-2, 140, 157, 162

Impact of Manual Pb-Free Soldering Process 145

Impact of Repair 217-18

Incorporating Pb-free 142-3

Industrial Advisory Board see IAB

industry ii-iii, 2, 9-10, 12, 46, 55, 66, 75, 77, 109, 111, 119, 142, 256, 284

industry documents 25, 170, 176, 179

Industry Pb-Free Electronics Best  
Practices Forum 285

industry practices 188, 226, 228, 259, 261

Industry Standard 62-3, 167, 180, 183, 186, 188, 220-1, 232, 258-9

Industry Standard Test 192, 203, 210-11, 261-2, 268, 270, 272

iNEMI Pb-free reliability study 124

inert atmosphere 144-5, 148, 152

inspection 58, 120, 160, 216-18

inspection requirements 24, 161

Interconnect Stress Testing (IST) 187-8, 234, 259

interconnections 52, 194, 196, 204, 244, 273-5

Interconnects Containing Pb-free Solder and Finishes 22, 207, 269

intermetallic bond 226-7, 233

internal Pb-free solders 20

introduction 26, 71-2, 169, 172, 239, 251, 282

Introduction of Pb-free materials 42, 166

IPC 10, 29, 53, 80, 118-20, 124, 128, 183, 208, 236, 256, 258-9, 270

IPC-9701 206, 209, 221-2

IPC-A-610 72-3

IPC-SM-785 184, 206-7, 232, 269

IPC-TM-650 79, 183-5, 187, 191, 201, 204, 210-11, 235, 238, 258-9, 261, 266, 268, 272

isothermal 192, 199-200, 202-3, 261-2, 265, 268, 275, 278

isothermal aging 209, 211, 231, 270

IST (Interconnect Stress Testing) 187-8, 234, 259

## J

J-STD-001 32, 35, 41-2, 72, 76, 174, 177, 180

Japanese Electronics Industry Association (JEITA) 124

JCAA (Joint Council on Aging Aircraft) 10-11, 23

JEDEC 185, 190, 258

JESD 65, 69, 106, 108, 190

joint geometries 55, 81, 194, 202, 267-8, 272

## K

key design considerations 18, 21

## L

laminates 77, 79, 98, 117, 183-4, 186-7, 235, 237, 259

laser soldering processes 151-2

layers, plated 34

LEAP 9-10, 283

levels

- joint 236
- moisture sensitivity 21, 23, 64, 66, 118

LFCP 27-9, 31-2, 167, 169, 172, 176

life models 55-6

line replaceable unit see LRU

Linear Thermal 200-1, 266

liquid 131-2, 134, 191, 261

load train 202, 267-8

loads 26, 217, 228, 231, 253

- sustained 231-2, 253

logistics ix, 22, 42, 166, 171-2, 245, 284

logistics management 172, 174, 245

long-term fatigue performance of Pb-free solder interconnections 194, 272

Low Expansion Alloy 68-9

LRU (line replaceable unit) 40, 45, 48, 50, 53, 73, 98-9

## M

mainstream Pb-free solders 220, 223-5, 235

Manhattan Project Team 243

Manual Pb-Free Soldering Process on Soldering Iron Tips 145

manual soldering 120, 144

Manual soldering operators 144, 151

- manufacturability 21, 83
- manufacture 44-5, 101, 165, 214, 217-18, 232, 239
- manufacturers 33, 44-5, 62, 81-2, 99, 170, 282
- manufacturing iii-iv, 14-15, 19-21, 27-8, 31-2, 59-60, 62-6, 75-7, 83, 111, 114-63, 166, 215-17, 219, 251-3
- manufacturing floor 122
- manufacturing flow 114-15, 143, 243
- manufacturing gaps 250
- manufacturing Pb-free CCAs 183
- manufacturing practices, best Pb-free 254
- manufacturing process temperatures 19, 250
- manufacturing process test coupon 109
- manufacturing processes 2, 18, 21, 49, 66, 74, 102, 114, 116, 219, 244
- Manufacturing processes for Pb-free assembly 118
- manufacturing requirements 32, 41
- Manufacturing Technical Data Packages 111
- manufacturing technology ii, iv
- manufacturing technology gaps 248
- markets, similar 62, 66, 70-1, 74, 77, 81-2
- marking 43, 119, 174
- material compositions 169, 220, 245
- Material properties of mainstream Pb-free solders 223
- material solutions 71-2
- Material Testing for Computational Modeling ix, 194, 272
- Materials Analysis and Incoming Inspection of External Package 186, 189, 258, 260
- Materials Requirement 32
- Matte Sn 68-9
- mean time between failure (MTBF) 66, 217
- Measuring Whisker Growth on Tin and Tin Alloy Surface Finishes 190
- Mechanical 76, 195-6, 203, 208, 217, 268, 270, 274
- mechanical parts 61-3, 66-7, 82, 251, 295
- mechanical properties 97, 99, 196, 198-9, 202-3, 209, 274-5, 278
- Mechanical routing 153
- mechanical shock 1, 35, 49, 74-5, 98-9, 103, 182, 208, 211, 230-1, 235, 246, 270
- Mechanical Shock Testing 208
- melting temperature 9, 126-8, 132, 138, 142
- Metal-to-Metal 203, 267-8
- metal vapor arcing 38, 82-3, 85-6
- Metallic Materials 197, 262-5, 275
- metallographic cross sections 195-6, 202-3, 276-8
- metallurgy 209, 213
- Methods and Qualification Requirements for Surface Mount Solder Attachments 207, 269
- micro-sectioning 201, 266, 268
- microstructure 19, 97, 132, 134, 142, 195-6, 199-200, 204, 220, 274, 310-11
  - ending 196, 198-200
  - joint 126, 129, 131, 279
  - mixed 134-5
  - starting 274-7
- microstructure size scale effects 196, 202, 262-5, 267-8
- middle 80, 136
- MIL-HDBK-217 55-6, 109-10, 214
- MIL-STD-810 46, 49, 51, 225, 230
- MIL-STD-810 pyro-shock loading of Pb-free assemblies 94
- MIL-STD-810G 49, 184, 205-8, 268-70
- MIL-STD-1580 186, 189, 258, 260
- military 33, 36, 43, 190, 247, 261, 282, 285
- Miner's rule 89-90, 96-7
- minimum reflow temperature 126
- mitigate iii, 2, 9, 22, 57, 59, 62, 79, 165-6, 239, 244, 248, 281, 284
- mitigation effectiveness 109
- mitigations 29-30, 57, 78, 81, 224, 239

Mixed Solder Rework Temperature Profiles 24

Mixed Solders 132, 220, 229

Mixing of Pb-free solder 229

model predictions, computational 195, 204, 274-5

modeling ii, 45, 67, 95, 103, 194, 272, 296

models 16, 44, 55-6, 95, 97, 99, 101, 108-9, 182, 194-5, 217-18, 220-3, 231-5, 239, 274-5, 279  
mathematical 269-70

modifications 151, 187, 191, 195-7, 199-201, , 213, 215, 244, 251-2, 259, 261-6

Modulus 197, 263

Moisture Sensitivity Level see MSL

MPa 89, 188, 231, 260

MSL (Moisture Sensitivity Level) 21, 23, 64, 66, 118

MTBF (mean time between failure) 66, 217

## N

National Center for Manufacturing Science (NCMS) 124

National Institute of Standards and Technology see NIST

N<sub>f</sub> 89, 221-2, 224, 280

Ni 69, 125, 130, 135, 140, 226

NIST (National Institute of Standards and Technology) 10

NL-1 279

NL-2 279-80

## O

OEMs (Original Equipment Manufacturers) 1-2, 6-7, 9, 56, 114, 120, 125, 169

Office of Naval Research see ONR

ONR (Office of Naval Research) i, iv-v, 9, 283

Operational Requirements Document (ORD) 27-8

operator training 120, 158, 173, 175, 177-80, 245

Original Equipment Manufacturers see OEMs

## P

package-on-package Pb-free solder 273

packages, technical data 44, 111, 119

pad cratering 38, 54-5, 86-7, 94, 158, 162, 183, 193, 210-11, 218, 221, 224, 226-7, 235, 272

part finishes 20, 26, 28, 62, 66, 112, 165, 168, 171, 173

parts screening 122

Paste Solderability Testing 191

pastes 128, 185, 191-2, 194, 258, 261

Pb 1, 6, 17, 31, 35, 129, 133-4, 142, 229, 238

Pb-free i, 1, 6-7, 25-7, 37-9, 43-5, 52-5, 61-3, 70-2, 77-9, 82-5, 116-18, 120-3, 126-7, 129-30, 157-8, 166-70, 174-8, 185-92, 195-201, 203-11, 243-6, 258-72  
incorporation of 43, 171  
introduction of 63, 70  
tested 88

Pb-free A&D 194, 245

Pb-free alloys 35, 40, 43, 46-7, 72, 74-5, 93, 95, 97-8, 118, 120, 140, 143, 178, 194, 204  
common 75  
multiple 35, 41  
preferred 55, 75

Pb-free and SnPb alloys 95

Pb-free and SnPb-based products 58

Pb-free and SnPb solders 229

Pb-free assemblies 14, 43, 53, 55, 71, 79, 83-4, 86, 112, 114, 118, 121-2, 159, 163, 172, 245-6  
repairing 173  
reworking 238

Pb-free assembly process 39, 235, 240

Pb-free ball 130

Pb-free BGAs 73, 125, 229

Pb-free BGAs in SnPb solder 142

Pb-free CCAs 78, 119, 163, 183, 193

Pb-free changes 36, 168-9

Pb-free components 1, 30, 43, 58-9, 73, 142, 190  
assembling 126

- Pb-free components in SnPb assembly 143
- Pb-free considerations 37, 85
- Pb-free Control Plans 28, 30-1, 43, 45, 56, 120, 173
- Pb-free design considerations 23, 100
- Pb-free design rules 100, 103
- Pb-free design stress levels 87
- Pb-free designs 18, 86
  - complete 84
- Pb-free electronics i, iii-iv, viii, 1-2, 4, 7-9, 11-12, 22, 44-5, 56-7, 59-60, 165-6, 172-3, 176-7, 182-3, 250-2, 283-5
  - introduction of 168, 170-1
  - manufacture 120
- Pb-free electronics challenges 12, 283
- Pb-Free Electronics Cultural Issues viii, 12
- Pb-free electronics in A&D products 2, 250
- Pb-free electronics issues 9, 11
  - multiple 12
- Pb-free electronics manufacturing ii, 114, 117, 289-90, 294-5
- Pb-free electronics manufacturing
  - certifications, third-party 120
- Pb-free electronics manufacturing process 248
- Pb-Free Electronics Reliability 182, 194, 296
- Pb-free electronics reliability models 248
- Pb-free Electronics Risk Management see PERM
- Pb-free electronics usage iii, 247
- Pb-free failure modes 38, 40, 56, 70
- Pb-free failure modes and Pb-free models 51
- Pb-free field issues 170
- Pb-free finishes 28, 34, 62, 78, 180
- Pb-free Finishes for Components Used in High-Reliability Products 67
- Pb-free fluxes 153
- Pb-free impacts 26, 100, 112, 170, 177
- Pb-free interconnect technologies 39, 84
- Pb-free interconnection designs 103
- Pb-free interconnection reliability 272
- Pb-free interconnections 49, 56, 98-9, 102, 273
  - fatigue of 98, 102
- Pb-free issues 43, 109, 167, 172
  - addressing 165, 173-4
  - customers control 167
- Pb-free joints 130, 162
- Pb-free manual soldering 144, 158
- Pb-free manual soldering processes 152
- Pb-free manufacturing 11, 57, 121, 282
  - efficient 120
- Pb-free manufacturing for A&D 184, 191
- Pb-free manufacturing of high reliability electronics 121
- Pb-free material behaviors 50, 54, 246
- Pb-free material properties 18, 54
- Pb-free materials 4, 6-7, 9, 14, 47, 51, 66, 100, 120, 167-9, 180, 205, 231, 237, 243-6, 251
  - introduction of 213
- Pb-free mitigation ii, 10
- Pb-Free Overview viii, 4, 7-12
- Pb-free parts 10, 62, 67-8, 81, 122, 172, 229, 238
- Pb-free PCB reliability 80
- Pb-free performance 45, 230
- Pb-free processes 6, 78, 83, 121, 137, 144, 187, 244, 257
- Pb-free processing 114-16, 120, 143
- Pb-free product development process 238
- Pb-free production hardware 182, 206-8
- Pb-free products 7, 57, 119, 215, 228, 243
- Pb-free qualification requirements 53
- Pb-free reliability 102, 187, 246
- Pb-free reliability issues 183
- Pb-free reliability knowledge 54
- Pb-free repair 84, 179
- Pb-free repair alloys 178
- Pb-free requirements 170-1



- Pb-free rework 43, 84, 158-9
- Pb-free risk assessment 40, 111
- Pb-free risk management 25, 27-8, 30, 61, 71
- Pb-free risk mitigation 29, 71
- Pb-free risks 26, 28, 32
- Pb-free SAC solder alloys 146, 148
- Pb-free solder 21, 75
- Pb-free solder alloys 22, 49, 59, 68, 72-3, 124-5, 145, 147-8, 150, 152, 175, 178-9, 185, 194, 204, 209
- Pb-Free Solder Alloys Applicable Processes 125
- Pb-free solder alloys melt 145
- Pb-free Solder and Finishes 52
- Pb-Free Solder and Mixed Metallurgy Modeling 23
- Pb-free solder and Pb-free surface finishes 14
- Pb-free solder assemblies 85-6, 233
- Pb-free solder attachment processes 109
- Pb-free solder attachments 227, 229
- Pb-free solder balls 131
- Pb-free solder change 95
- Pb-free solder equivalents 81
- Pb-free solder fatigue 56
- Pb-free solder fatigue models 52
- Pb-free solder interconnect reliability 222, 229
- Pb-free solder interconnection failure 87
- Pb-free solder interconnections 22, 98, 101, 103, 194, 204, 272-3
- Pb-free solder interconnects subject 223
- Pb-free solder joints 9, 72, 98-100, 103, 137, 153, 156-7, 192, 203-5, 228, 233, 278
- Pb-free solder laminate and PCB finish 81
- Pb-free solder manual process training 156
- Pb-free solder manual process training and Pb-free workmanship standards training 157
- Pb-free solder microstructure 18
- Pb-free solder paste 138
- Pb-free solder process readiness 120
- Pb-free solder processes 116, 119  
implementation of 116, 118, 154-5, 160, 162-3
- Pb-Free Solder Processes Impacts 144
- Pb-free solder properties 53, 87
- Pb-free solder sample preparation steps 276
- Pb-free solder specimen size 204
- Pb-free solder stress design rules 21
- Pb-free solder success 47
- Pb-free solder termination loads 20
- Pb-free soldering 142-3, 151  
implementation of 123-4
- Pb-free soldering operations 234-5  
elevated 234
- Pb-free soldering processes 118, 121, 124, 136, 144, 150-1, 156  
implementation of 156, 161
- Pb-free solders 14, 28, 39-40, 42, 47, 52-3, 55, 74-6, 83-7, 124-6, 128-32, 177-8, 219-20, 224-30, 245-6, 277-8  
applicable finishes 180  
computational 53  
conforming 35  
implementation of 145-7, 149  
introduction of 47, 71  
molten 312  
newly-developed 204  
selected 252  
thermal fatigue resistance of 233  
wetting 144
- Pb-free solidification 142-3
- Pb-free surface finishes 182, 185, 193-4
- Pb-free surfaces 175-6, 179
- Pb-free technology 30, 39, 62, 71, 73, 111
- Pb-free test 103
- Pb-free test vehicles 205-9
- Pb-Free Tin Finish 16-18
- Pb-free tin plating 62-3
- Pb-free tin surface finishes 67
- Pb-free transition 172, 183, 244, 246

- Pb-Free Updates Urgently Required 42, 166
  - Pb-free vapor phase equipment 150, 152
  - Pb-free wave solder baths 149, 152
  - Pb-free wave solder joints 136
  - Pb-free Wave Solder Profile 149
  - PCB Artwork and Design Considerations for Pb-Free Solder Applications 24
  - PCB CAF Testing 187
  - PCB Copper Test 188, 260
  - PCB Delamination 186-7, 259
  - PCB design 21, 67, 77-8
  - PCB Materials and Manufacturing for Pb-free CCAs 184
  - PCBs (printed circuit board) 18, 20, 24, 27-8, 45, 61-2, 71, 73, 77-80, 99, 116, 185-7, 190, 193-4, 196, 198, 233-6, 258-9, 261
  - peak reflow temperature 80, 126, 257
  - PERM (Pb-free Electronics Risk Management) 11-12, 167, 254, 256
  - perspective 10, 12, 218, 290-1
  - pervasive issues 6, 9, 254
  - Phenolic 80
  - plated through hole see PTHs
  - Plating Materials Using X-Ray Fluorescence Spectroscopy 186, 189, 258, 260
  - polycrystalline 265-6
  - polycrystalline grain size 265-6
  - Potential mixing of disparate Pb-free solders 229
  - PPL (preferred parts list) 27-8, 62-3, 65-6, 250
  - predictions 108-10, 215, 226, 228, 236, 246, 279
  - preferred parts list see PPL
  - printed circuit board see PCBs
  - printed wiring boards (PWB) 184, 218-9, 235, 237, 251, 293
  - process qualifications 120-1, 153, 214
  - processing temperatures, higher 28, 39, 137, 151-2
  - procurement 22, 28, 31, 33, 104-5, 159
  - product design iv, 6, 39, 59, 98-9, 167
  - Product Design and Development 3, 293-5
  - product development 45, 97, 100, 103
  - product development cycle 14-15
  - product life cycle 3-4, 111, 166, 169, 213, 243, 245
  - Product Life Cycle Diagram 3
  - product reliability 1, 7-8, 165, 214, 247
    - reduced 58, 176
  - Product Reliability Risk Factors
  - Product Sustainment 8
  - product sustainment 3, 7, 14, 59, 294-6
  - production 22, 36-7, 49, 59, 100, 102, 111, 115, 165-6, 176-7, 240
  - production hardware 184, 205-9, 269-70
  - production readiness reviews 111
  - products
    - adhesive 124
    - consumer 14, 106
    - finished 175-6, 179
  - profiles, conventional SnPb 134, 140
  - properties 18, 95, 184, 191, 199-200, 203, 220, 232, 262, 267-8, 277, 279-80, 282
    - physical 194-5, 204-5, 213, 273-4
  - protocols, tin whisker risk mitigation 160-1
  - PTH reliability 83-4, 183
  - PTHs (plated through hole) 18, 24, 38, 54, 73, 80, 109, 116-17, 234, 241
- ## Q
- qualification 22, 36, 47-8, 52-4, 63, 73, 77, 79, 97-9, 102-3, 169-70, 182-3, 194-5, 225, 239, 269-70
  - Qualification Best Practices Testing 294-6
  - qualification goal 48
  - qualification requirements 49-50, 53, 71, 102, 207, 269
  - qualification standards 183, 185, 190, 192-3

qualification test parameters 49, 101-3  
 qualification test requirements 27, 48, 54, 103  
 qualification tests 48-50, 54, 103, 182, 190, 205, 221  
   design hardware 211

## R

ramp rates 95, 206, 279-80  
 rates, cooling 76, 130, 142-3, 230, 279  
 Raytheon 161  
 R&D 281, 283  
 recently-received assemblies 45  
 recommendations 4, 25, 54, 62, 72, 84, 250, 253, 288  
   cognitive design 250  
 reflow 20, 72, 74-5, 118, 121, 130-4, 143-4, 151-2, 192, 237, 257  
 reflow soldering 119, 145  
 reliability 3-4, 7, 10-11, 14-15, 44-5, 55-6, 62-6, 72, 75, 95-6, 112, 166, 174-6, 179-80, 192-4, 213-41  
   predicting 109  
   system 30, 32, 193  
   system level 216-17  
 Reliability and Life Requirements 27, 55  
 reliability data iv, 18, 20, 28, 55  
 reliability degradation 173-4  
 reliability failures 60, 215  
 reliability issues 210, 225, 272  
   potential product 119  
 reliability modeling 109, 282  
 reliability models 56, 108, 222, 248  
 Reliability of internal Pb-free solders 20  
 reliability predictions 109, 214  
 reliability programs 213-14, 223  
 reliability requirements 35-6, 55, 112, 179, 213, 248  
 reliability risks 7, 56, 140, 165, 169, 229, 232  
   greatest 182  
   primary product 7  
 reliability test 95, 97  
 Reliable Solder Joint 127, 143  
 repair ix, 20-2, 24, 42-4, 57, 73-4, 83, 112, 165-6, 172-3, 176-8, 180, 217-18, 229, 236-7  
 repair activities 83, 176, 180, 218, 229  
 repair alloys 36, 176, 179  
 repair analysis 172-4  
 repair capabilities 179  
 repair costs 44, 58-9  
 repair depots 43, 252  
 repair documentation 176-7, 245  
 repair facilities 165, 174-8, 180, 252  
 repair of A&D assemblies 174-5, 177-8  
 repair Pb-free assemblies 175-6, 179  
 repair procedures 112, 165, 173, 175, 177-80  
 repair processes 1-2, 19, 42-3, 59, 101, 166, 172-6, 178-80, 236  
 Repair shops 171, 176  
 repair solder alloys 21, 32, 72, 112, 180  
 Reprocessing of Pb-Free Components to SnPb 60  
 requirements viii, 3, 15, 20, 27, 41-5, 47-8, 51-5, 61, 72-3, 99, 101-2, 109-10, 166-70, 189, 260-1  
   safety 36-7  
 requirements coordination 169-70  
 Requirements for Soldered Electrical and Electronic Assemblies 183  
 research iii, 9, 32, 35, 59-60, 90, 94-5, 97, 223, 225, 231, 243, 247-8, 253, 283  
 Research Coordination Task Team 256  
 resistance 189, 191, 236, 260-1  
 Resistance Test 187, 258-9  
 Restriction of Hazardous Substances see RoHS  
 review 35, 37, 41, 71, 73, 83-4, 103, 156, 176, 178-9, 284-5, 287-8, 290-1  
   critical design 84, 100  
 rework ix, 1, 8, 19-22, 24, 29, 44, 57-60, 74-5, 143-4, 158, 217-18, 229, 233-4, 236  
   manual 158

rework processes 159, 245, 251

Rework Time 159

risk factors 7-8, 39

risks iii-iv, 1, 7-9, 11-12, 66-7, 71, 75-6, 78-9, 105-6, 165, 176, 217-18, 232-3, 237-9, 245-7, 284

greatest 78

increased 17-18, 66, 237

low 18, 21, 31, 75-6

Roadblocks 293-6

roadmap 2, 12, 248, 281, 283

RoHS (Restriction of Hazardous Substances)

6, 11, 33-5, 125, 282

RTCA-DO-160 52

RTCA-DO-254 52

## S

SAC 16-18, 55, 72, 74-7, 89, 92-3, 124-5, 128-30, 140-3, 158-9, 185, 219, 221-2, 224-5, 231, 253

SAC alloys 126, 137-8, 143, 253, 278

SAC solder ball 132

SAC solder joints 209, 262

SAC solders 130, 208, 220, 226, 230-2

mainstream 232, 235

safety systems 27, 36-7

sample geometries, smaller 196, 262-5

sample geometry 196, 199-200

Sample of Pb-free electronics issues 9

sample size 265-6

scale, microstructure size 263, 265-6

scanning electron microscopy (SEM) 51, 122, 186, 189, 201, 203, 258, 260, 276, 278

schedule 54, 100, 103, 111, 272, 282, 284-5, 288-91

scope ii, 11, 23, 32-3, 166-7, 284

screen 101, 122, 217-18

selection 72-3, 79, 237, 251, 253, 281-2, 284

SEM see scanning electron microscopy

SEMP (systems engineering management plan) 27-8, 30, 32, 34-5, 44, 103

sensors, equipment temperature 150, 152

service ii, 21, 47, 50, 58, 196, 227, 230, 274-5, 278-80

service conditions 45, 95-6, 202, 223, 228, 236, 277-80

service life 20, 50-1, 101, 216-17, 234

service life conditions 49, 53, 98-9, 101, 211

Service Life Model 16-17

service lifetimes 49, 98-9, 182, 194-5, 273-4

shared mental model 289

Shear 203, 267-8

Shipping and Handling Procedures 175, 177-9

shock 14, 16-17, 19, 21, 23, 26, 30, 50-2, 86-7, 90, 96-7, 108-9, 217-18, 226-7, 229-32, 236  
explosive 90-1  
functional 90-1

shock performance 72-3, 94-5, 226

shock pulse 208, 270

Shock Response Spectrum (SRS) 208, 222, 270

Shock Test Guidelines for Solder Joint Reliability 208, 270

Shorts 217-18

shrinkage voids 132, 136-7, 142, 144

Simulated Solder Joint Testing 201, 203, 276

simulated solder joints 195, 203-4, 274, 277-8

SIR (Surface Insulation Resistance) 191, 238, 261

size scales 196, 199-200

SME team 281, 284, 288, 290-1

SMEs (Subject Matter Expert) v-vi, 247, 254, 284-6, 288, 290-3

Sn 124, 128, 130, 132-5, 139

Sn60 solder 191, 261

SnAgCu Ball 133

- 
- 
- SnAgCu solder ball 132
- SnPb 14, 16-19, 35, 47, 56-7, 61-2, 72, 76-7, 95, 127-30, 132-3, 141-3, 221, 224-5, 228-30, 244-6
- SnPb and Pb-free alloys 138
- SnPb and Pb-free alloys comparisons 139
- SnPb and Pb-free soldering process flows 119
- SnPb and Pb-free soldering processes 119
- SnPb assemblies 14, 43, 51, 87-8, 127, 171, 234
- SnPb-based components 58
- SnPb design rules 66
- SnPb designs to Pb-free solder 78
- SnPb eutectic solder alloy 18
- SnPb products 215, 228
- SnPb solder 9, 20, 25, 30, 34, 56, 73-4, 130, 143-4, 175, 178, 180, 219-20, 222-3, 229, 232
- SnPb solder alloys 66, 118, 145-6, 148-9
- SnPb solder and Pb-free components 57
- SnPb solder and Pb-free solder 130
- SnPb solder assemblies 125, 219
- SnPb solder balls 57
- SnPb solder interconnects 219, 224
- SnPb solder paste 125, 140, 142
- SnPb solder process 118, 229
- SnPb soldering 129, 144
- SnPb soldering process 41, 121, 125
- SnPb to Pb-free manufacturing technology 120
- SnPb to Pb-free solder 84
- SnPbAgCu Mixed Solder 133
- solder 6-8, 16-19, 61-3, 66, 74-5, 81-2, 114, 127-30, 132-4, 136, 179-80, 224-7, 231-2, 267-9, 272-5, 279-80
- bulk 99, 129, 136
  - designed 180
  - free 10-11, 25-6, 221, 280
  - hot 57-8, 62, 66
  - reliable 126
  - simulated 202-3, 277
  - tin-lead 26
- solder alloy changes 91, 170
- solder alloy materials 35, 119
- solder alloy melting temperature 146
- solder alloy requirements 118, 169
- solder alloys 21, 23, 32, 35, 41, 74, 99, 112, 119, 165, 172, 176, 178, 191-2, 196, 262-5
- alternative Pb-free wave 142
  - free 10, 26
  - managing Pb-free 82
  - stream Pb-free 226
- Solder Alloys Reflow 76, 125
- Solder and PCB material properties 98, 103
- Solder Attachments 53, 294
- solder balls 140, 210, 223, 272
- diameter of 210, 272, 279
- solder compositions 196, 199-200, 220, 275-7
- solder cools 130
- solder defects 38, 130, 156
- solder dip 186, 259
- solder dressing characteristics, improved 148, 152
- solder failure 90, 94
- solder fatigue 55-6, 90, 95
- Solder Fatigue and Interconnect Reliability Analysis 86
- solder fountain 74, 77
- solder interconnections 219, 229
- solder interconnects 219-21, 232
- defective 220
- Solder Joint 73, 120-1, 132, 153, 162, 193, 195, 202, 204, 209-10, 217, 224, 228-9, 232, 244, 277
- design limits of Pb-free 98-100
  - inspecting Pb-free 155
  - simulated Pb-free 201, 276
  - unacceptable 140
- Solder Joint Formation viii, 124
- Solder Joint Reliability Considerations 23
- Solder Joint Tin Whisker Assessment 192
- solder mask 77, 230, 235

- solder materials 32, 35, 44, 74, 83, 101, 119
- Solder Metallurgy viii, 124
- solder paste 121, 125, 128, 183, 191-2, 261
- solder paste deposition viii, 123
- solder paste handling 123
- Solder Processes viii, 143
- solder repair alloys 36
- Solder Selection 27, 74
- solder stencil designs 67
- solder stress levels 76, 87
- Solder Testing 191
- solder tips 175, 178
- solder type 191, 261
- solder volume 67, 222
- solderability 20, 78, 83, 116, 122-3, 168, 175-6, 179-80, 184-5, 189, 258, 260, 282
  - paste 191, 193-4, 261
- solderability of electronic component 189, 260
- solderability plating 79
- Solderability Tests 260
- Solderability Tests for Component 189
- Solderable Finish 68-9
- Soldered Electrical 183, 313
- soldering 39, 41, 59, 77-8, 120, 128, 151, 282
- soldering, selective 150-1
- soldering iron tips 145
- soldering materials 62, 185, 251, 258
- soldering process 77, 128, 143, 150, 153
- Soldering Resistance of Modifications 187, 259
- Spares contracts 168-9, 173-4
- Specimen geometry 265-6
- SRP (Stockpile Reliability Programs) 10
- SRS (Shock Response Spectrum) 208, 222, 270
- stabilization 195, 262, 274
- Standard 22, 33-4, 51-3, 196-7, 199-201, 262-6
- Standard Test 197, 203, 263-4, 267
- Standard Test Methods 183, 267-8
- standardized test methods 210, 272
- standards 1, 7, 9, 29, 37, 43, 46, 63, 105, 122, 167, 170, 183, 193, 211, 214
- stencil 123
- Stockpile Reliability Programs (SRP) 10
- storage 16, 45, 121-4, 149, 154, 173-4, 177
- storyboards 281, 286, 288, 290-1
- strain rates 195, 197, 199, 202, 230, 263, 274-7
- strain-time curves 195-6, 199, 274-5
- stress levels, design solder 21
- structured development process 281, 289, 291, 293
- sub-assemblies 10-11, 97
- sub-teams 281, 283, 285-6, 288-92
- Subject Matter Expert see SMEs
- substrates 114, 251, 273-5
- suppliers 1, 6, 22, 25, 28, 30, 34, 41, 45, 47, 61-2, 69, 167, 169, 176, 226
- supply chain 1-2, 42-3, 63, 84, 112, 168, 172, 243
- Surface Finish 24, 64-5, 186, 189-90, 258, 260
- Surface Finish Verification 186, 189
- surface finishes 32, 59, 82-3, 122, 184, 190, 193, 238, 261
- Surface Insulation Resistance see SIR
- Surface Mount Solder Qualification Testing 207
- Surface Mount Technology Association see SMTA
- surface tension 128-9, 138
- sustainment iv, ix, 2, 4, 15, 18-19, 21, 27-9, 32, 42-3, 57, 59-60, 111-12, 165-80, 245, 252-3
- sustainment process control 64-5
- sustainment requirements 30, 32, 42
- system requirements 66, 168-70, 205, 207-8, 211

systems ii, v, 8, 22, 27-8, 30, 32, 34-5, 37, 39-40, 44-5, 51, 55, 165-6, 193-4, 215-17

Systems Containing Pb-free Solder 22

systems engineering management plan see SEMP

## T

Task Team 256

TC see temperature cycling

team iv, 215, 245, 247, 281-92  
high performing 281-2, 289, 293

team members 284, 287, 289-91

team process issues 288, 290

team selection 281, 283-4, 289, 293

technology ii, v, 7, 11, 26, 42, 64, 221, 250, 281, 292

temperature 19, 50, 63-4, 75, 77, 101, 118, 125, 127, 132, 140, 144, 149-51, 217-18, 232-3, 241  
higher 59, 117-18, 144, 151, 159, 187  
low 23, 230  
maximum 77, 118, 126, 230  
peak 128, 134-5, 147

temperature cycling (TC) 1, 23, 49-50, 74, 98-9, 103, 221, 224, 227, 232

temperature excursions 221, 233

temperature extremes 25, 95, 182, 205-6

Temperature Process Windows 241

Temperature Ratings 23, 64

temperature requirements 46, 175, 178

temperature sensitivity 118, 150, 240

temperature soldering irons 144, 152

tensile strength 188, 197, 235, 260, 264

Tension Loading 203, 267

term reliability, long 14, 162, 185, 247, 258

terminations 112, 173, 189-90, 260

test 3-4, 8, 41-2, 49-53, 59, 115, 186-8, 199-200, 205-9, 217-18, 223-5, 232-3, 238-40, 259, 269-70, 274-7  
accelerated 211, 280  
accelerated aging 98-9  
accelerated life 49, 99  
standardized 202, 204, 277  
step stress 225

Test and Applicable Standard 185-92, 195-201, 203-11, 258-61, 266, 268-72

test article 100, 209, 271

test conditions 193, 195-6, 202, 215, 226, 230, 245, 250, 262, 274-8  
accelerated 206-7, 269-70  
cited 106, 108

test environments 198-9

Test Equipment 40, 50, 174, 204, 206, 209, 258-72

test fixture 120, 196, 199-200

test method development 50, 54

Test Method for Linear Thermal 200-1, 266

Test Method Standard 51, 184, 191, 193

test methodologies  
design validation 99  
design verification 99

test methods 18, 49, 51, 53, 80, 98-9, 183-6, 188-93, 196, 199, 204, 225, 235, 238, 258-62, 264  
used 205-9

test parameters 98, 103, 182, 193, 204-6, 209, 211, 244, 251-2, 274, 277  
accelerated aging 49, 53, 98-9, 101

test regiments 274, 277-8

test results, accelerated 279-80

test specimen geometries 262-5

test specimens 196, 199, 201

test temperatures 145, 196, 198-9, 274-5, 277

test vehicle design 211, 252

test vehicles 10, 184, 205-11, 269, 272  
limited Pb-free 99

thermal cycle 16, 20, 35, 51, 206, 217, 278, 308

thermal cycling 14, 19, 25, 53, 73, 86-90, 94-5, 97, 106, 108, 134, 206-7, 209, 220, 229-30, 269

thermal gradients 138, 145, 257

thermal shock 95, 159, 206, 269

thermal shock cycling 206, 269

Thermomechanical Analysis 200-1, 265-6

thickness 65, 71, 160, 227, 267-8

time dependence 280

tin 22, 28, 41, 57, 65, 75, 81, 106, 122, 128, 190, 192, 233, 238-9, 282

tin avoidance 31

Tin-Lead Parts Pb-Free Parts Reason for Addition 64-5

tin pest 20, 75, 192-4, 217, 226, 233, 261

Tin Pest Testing 192

tin whisker acceptance 63, 104, 106

tin whisker growth 32, 54-5, 57, 104, 108-9, 194, 239-40, 246

tin whisker mitigation 11, 21, 28, 39, 67, 69, 73

tin whisker risk 17, 19-21, 28, 30, 32, 38, 68, 71, 73, 103, 108, 239-40, 251

Tin whisker risk assessment 64-5

tin whisker test methods 185, 192

tin whisker test requirements 69

tin whiskers 7, 22, 37-9, 41, 55-6, 58-9, 69-70, 106, 108-9, 160-1, 182-4, 192-4, 238-9, 246-7, 282

tombstone 138-9, 142

tombstoning 138-9, 220

Tooling Cleanup 121

tools 99, 105, 119, 144, 152, 209, 216, 244, 271, 296

topics 284, 288, 290, 292

trace failure 224-5, 236  
induced 224

traces 75, 136, 183, 225, 235, 238

training 9, 60, 116, 120-1, 144, 151, 174-5, 177-8, 251

transition i, iv, 1-2, 6, 9-10, 44, 56-7, 59, 74, 78, 82, 111, 116, 120-2, 124, 158

Transition to Pb-free Electronics 22

## U

underfill materials 71, 154-5

underfills 72, 115, 154-5, 217, 229-30

Underplate 68

Unovis 55, 131, 236, 278-80

## V

Validated computational models 182, 209, 211, 252

validation viii, 3, 15, 19, 83, 182-3, 194-5, 204-8, 225, 248, 269-70, 273-4, 294-6

variations 19, 28, 58, 72, 74, 76, 78, 140, 223, 232, 280

verification 102, 169-70, 182-3, 186, 189, 194, 204-8, 244, 258, 260, 269-70, 273, 294-6

Versa Module Eurocard (VME) 44, 173

vibration 16, 30, 46-7, 51, 72-4, 76, 81-2, 86-8, 90, 96-8, 108-9, 217-18, 224-5, 227-30, 235-6

Vibration and Shock Testing 25

vibration test 1, 52, 90, 270

Vibration Testing 207-8, 270

visual acceptance criteria requirements 156-7

VME (Versa Module Eurocard) 44, 173

voiding 137-8, 220, 227

voids 132, 137, 142, 211, 227

voltage 82-3, 218, 240



## W

warfighters ii, viii, 8, 182

Waste from Electrical and Electronic Equipment (WEEE) 6, 282

wave 74-6, 119, 125, 143-4, 149

wave solder 115, 137, 185, 219, 244, 258  
fountain 158

wave solder equipment 148-9, 152

wave solder process window 148, 152

wave solder processes, running Pb-free 149

wave soldering 73, 143, 147

weapons 8, 51

wetting 126, 128-9, 142, 144, 238

wetting time 128-9

whiskers 30, 40, 70-1, 79, 81, 104-6, 160-1, 238,  
240, 246, 250, 262, 282

## X

XRF 122-3, 174, 186, 189, 258, 260

“You cannot solve a problem from the same consciousness that created it.

You must learn to see the world anew.”

—*Albert Einstein (1879-1955)*





THE BENCHMARKING AND BEST PRACTICES  
CENTER OF EXCELLENCE